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Specification for 8.2"EPD

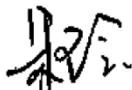
Model NO.: B082A05

Product VER: A0

Customer Approval

Customer	
Approval By	
Date Of Approval	

It will be agreed by the receiver, if not sign back the Specification within 15days.

Prepared By	Checked By	Approval By
		



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Version	Content	Date	Producer
A0	Initial	2025.08.06	Daisy



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1. General Description

B082A05 is a reflective electrophoretic E Ink® technology display module based on active matrix TFT substrate. It has 8.2" active area with 1440 x 1920 pixels. The display is capable to display images at 2 to 16 gray levels (1 to 4 bits) depending on the display controller and the associated waveform file it used.

2. Features

- 1440*1920 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Pure reflective mode
- Bi-stable display
- Commercial temperature range

3. Typical Application

eNote

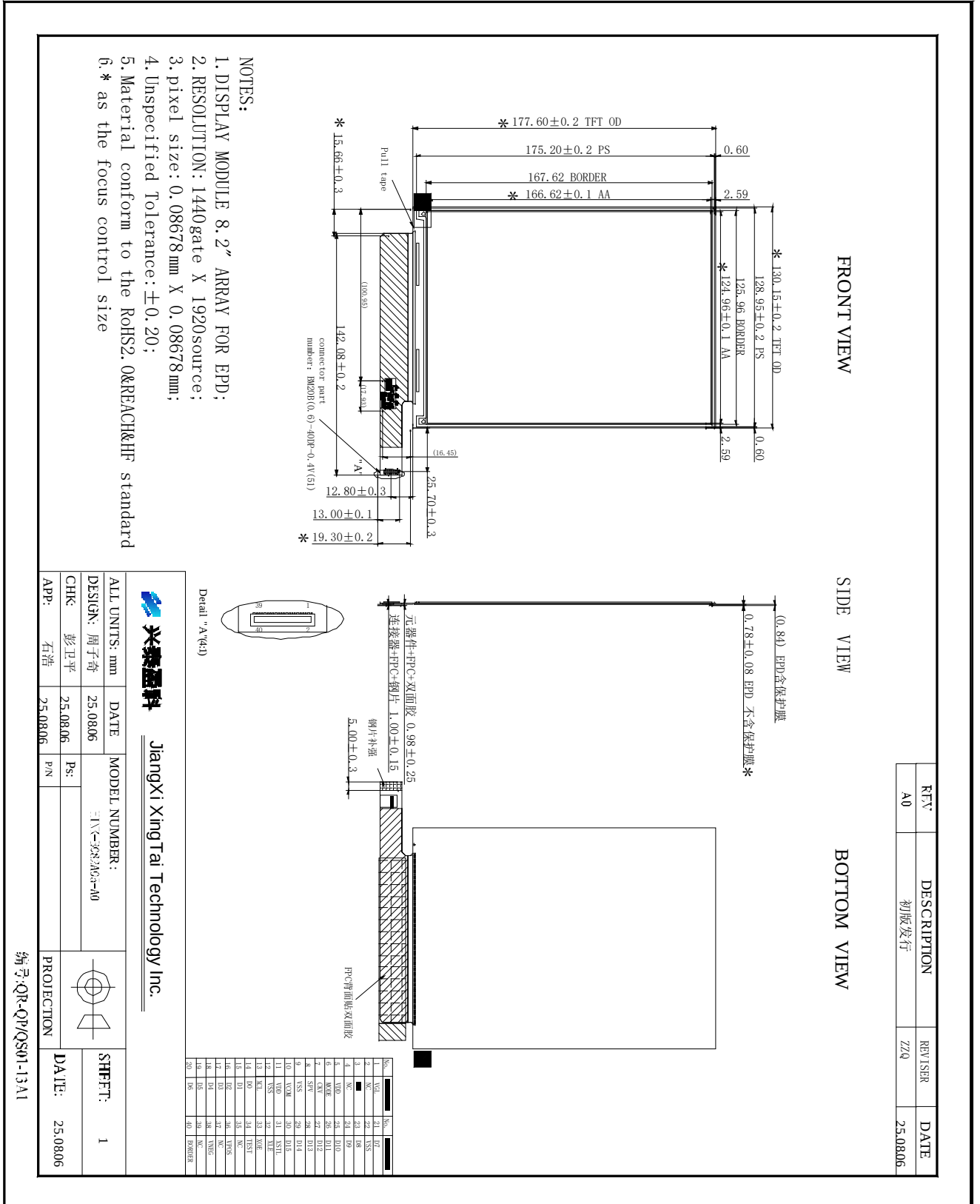
4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	8.2	Inch	
Display Resolution	1440(H)×1920(V)	Pixel	Dpi:292
Active Area	124.96 (H)×166.62 (V)	mm	
Pixel Pitch	0.0868×0.0868	mm	
Pixel Configuration	Rectangle		
Outline Dimension	130.15 (H)×177.6 (V) × 0.78(D)	mm	Without masking film
FPL	Carta 1300		
Weight	TBD	g	



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5. Mechanical Drawing of EPD module





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6. Input/output Terminals

6.1 EPD connector type

BM20B(0.8)-40DP-0.4V(51)

6.2 Pin Assignment of Panel

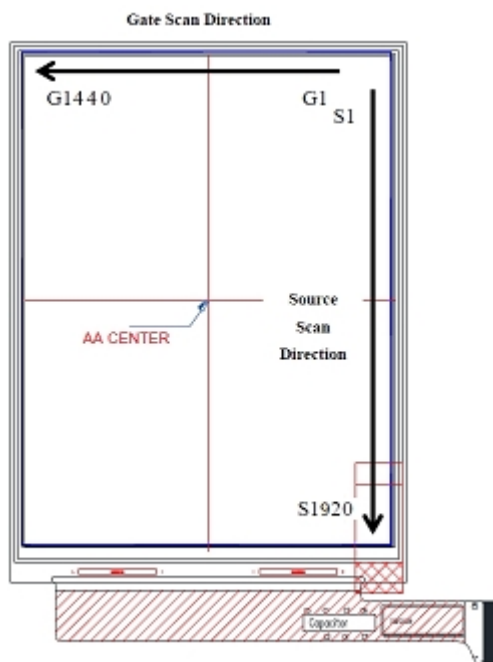
Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	NO Connection
3	VGH	Positive power supply gate driver
4	NC	NO Connection
5	VDD	Digital power supply drivers
6	Mode	Output mode selection gate driver
7	CKV	Clock gate driver
8	SPV	Start pulse gate driver
9	VSS	Ground
10	VCOM	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL	Clock source driver
14	D0	Data signal source driver
15	D1	Data signal source driver
16	D2	Data signal source driver
17	D3	Data signal source driver
18	D4	Data signal source driver
19	D5	Data signal source driver
20	D6	Data signal source driver
21	D7	Data signal source driver
22	VSS	Ground
23	D8	Data signal source driver
24	D9	Data signal source driver
25	D10	Data signal source driver
26	D11	Data signal source driver
27	D12	Data signal source driver
28	D13	Data signal source driver
29	D14	Data signal source driver
30	D15	Data signal source driver
31	XSTL	Start pulse source driver
32	XLE	Latch enable source driver
33	XOE	Output enable source driver
34	TEST	E Ink internal test pin (Note 1)
35	NC	NO Connection
36	VPOS	Positive power supply source driver



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37	NC	NO Connection
38	VNEG	Negative power supply source driver
39	NC	NO Connection
40	Border	Border connection

6.3 Panel Scan direction





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7. Display Module Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Logic Supply Voltage	VDD	-0.3 to +5	V	--
Positive Supply Voltage	VPOS	-0.3 to +18	V	--
Negative Supply Voltage	VNEG	+0.3 to -18	V	--
Max .Drive Voltage Range	VPOS -	36	V	--
Supply Voltage	VGH	-0.3 to VGL+50	V	--
Supply Voltage	VGL	-25 to +0.3	V	--
Supply Range	VGH-VGL	+10 to +50	V	--
Operating Temp. Range	TOTR	0 to +50	°C	--
Storage Temperature	TSTG	-25 to +70	°C	--

7.2 Display Module DC characteristics

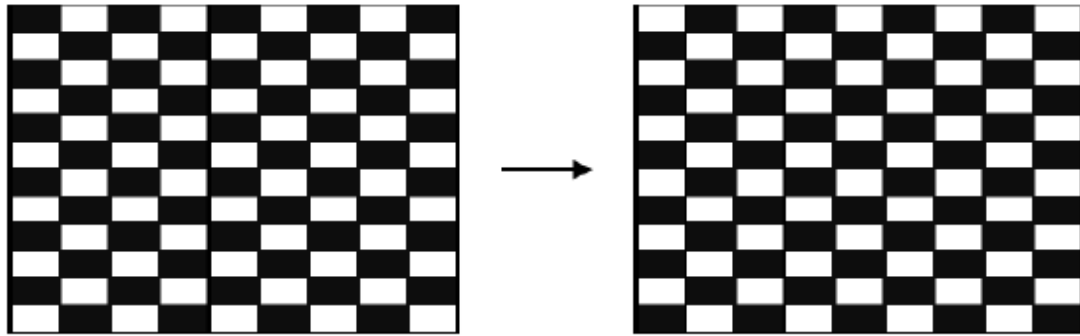
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	V _{SS}		-	0	-	V
Logic Voltage supply	V _{DD}		3.0	3.3	3.6	V
	I _{VDD}	V _{DD} =3.3V	-	12	15	mA
Gate Negative supply	V _{GL}		-21	-20	-19	V
	I _{GL}	V _{GL} = -20V	-	3	20	mA
Gate Positive supply	V _{GH}		27	28	29	V
	I _{GH}	V _{GH} = 28V	-	2	6	mA
Source Negative supply	V _{NEG}		-15.4	-15	-14.6	V
	I _{NEG}	V _{NEG} = -15V	-	2	200	mA
Source Positive supply	V _{POS}		14.6	15	15.4	V
	I _{POS}	V _{POS} = 15V	-	2	200	mA
Border supply	V _{COM}		-	Adjusted	-	V
Asymmetry source	V _{Asym}	V _{POS} +V _{NEG}	-800	0	800	mV
Common voltage	V _{COM}		-2.0	Adjusted	-1.0	V
	I _{COM}		-	1	-	mA
Panel Power	P		-	215.6	6608	mW
Standby power panel	P _{STBY}		-		0.17	mW



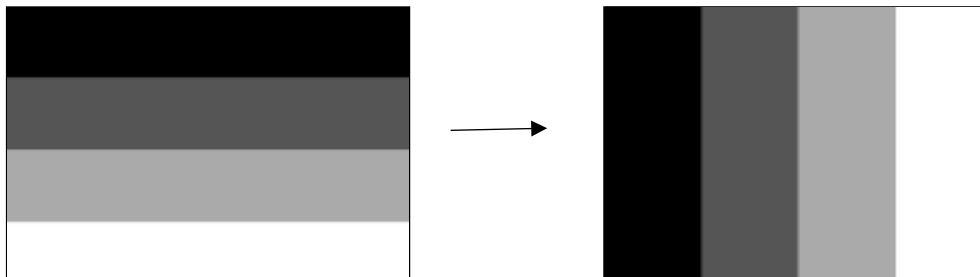
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Note.

1. The maximum average Currents for power consumption are measured at 25C by using 85 Hz waveform with the following pattern transition: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern.



2.The Typical power consumption is measured using 85 Hz waveform with following pattern transition: from horizontal 4 gray scale pattern to vertical 4 gray scale pattern.



- 3.The standby power is the consumed power when the panel controller is in standby mode.
- 4.The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by E Ink.
5. Vcom is recommended to be set in the range of assigned value ± 0.1 V
6. The maximum ICOM inrush current is about 0.8 A

7.3 Refresh Rate

	Min	Max
Refresh Rate	-	(85 Hz)

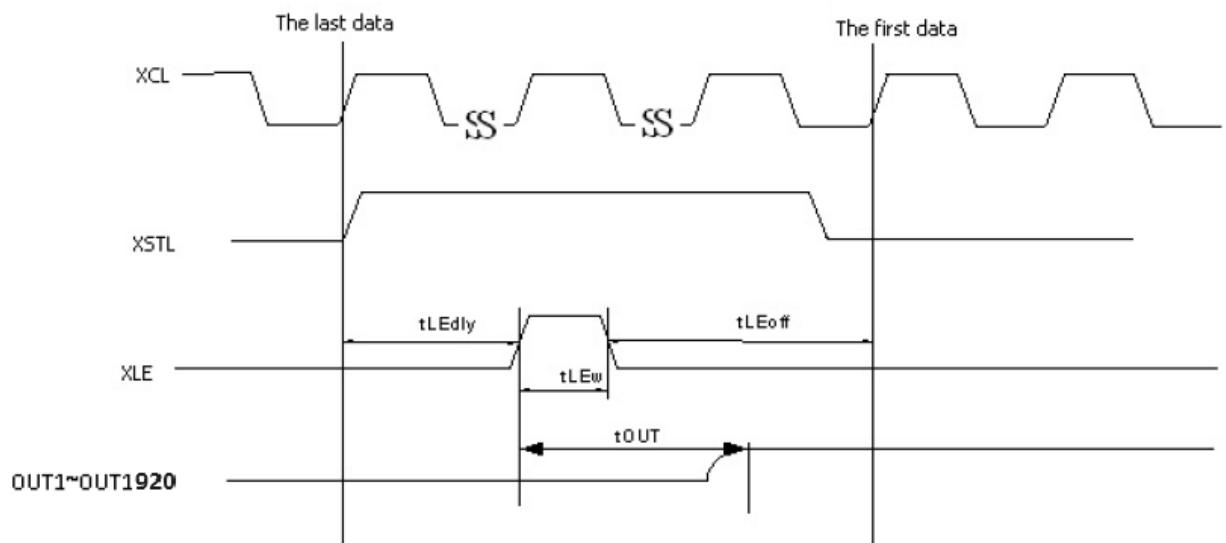


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7.4 Panel AC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	fckv	-	-	200	kHz
Minimum "L" clock pulse width	twL	500	-	-	ns
Minimum "H" clock pulse width	twH	500	-	-	ns
Clock rise time	trckv	-	-	100	ns
Clock fall time	tfckv	-	-	100	ns
SPV setup time	tSU	100	-	-	ns
SPV hold time	tH	100	-	-	ns
Pulse rise time	trspv	-	-	100	ns
Pulse fall time	tfspv	-	-	100	ns
Clock XCL cycle time	tcy	16.67	50	-	ns
D0 .. D15 setup time	tsu	8	-	-	ns
D0 .. D15 hold time	th	8	-	-	ns
XSTL setup time	tstls	0.5*tcy	-	0.8*tcy	ns
XSTL hold time	tstlh	0.5*tcy	-	240*tcy-tstls	ns
XLE on delay time	tLEdly	10.5*tcy	-	-	ns
XLE high-level pulse width (When VDD=3.0V to 3.6V)	tLEw	300	-	-	ns
XLE off delay time	tLEoff	200	-	-	ns
Output setting time to +/- 30mV(C _{load} =200pF)	tout	-	-	20	us

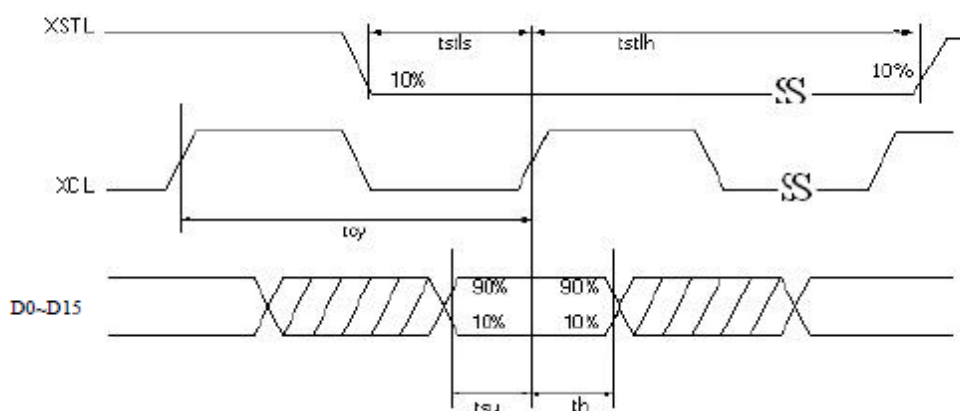
OUTPUT LATCH CONTROL SIGNALS



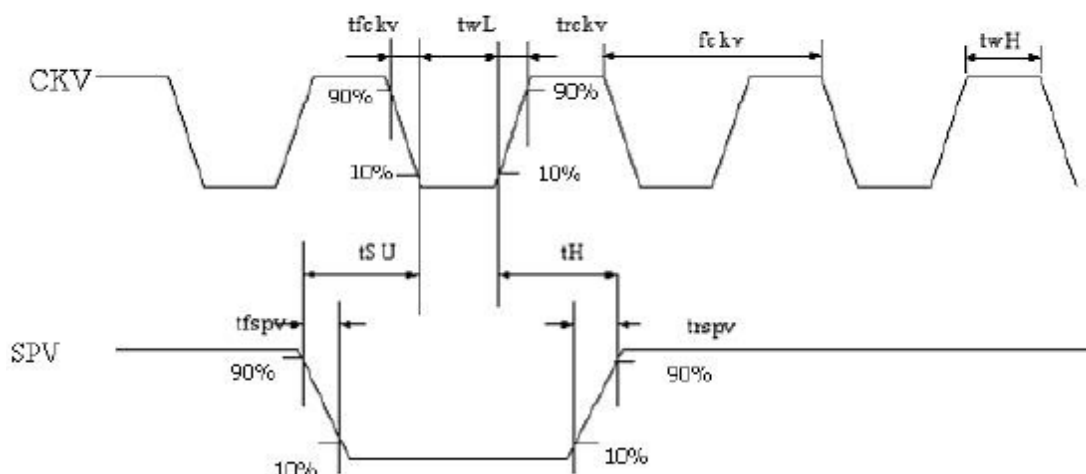


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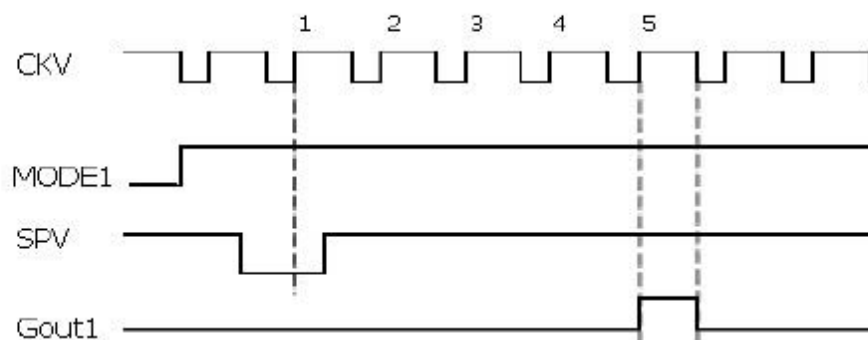
CLOCK & DATA TIMING



CKV & SPV TIMING



GATE OUTPUT TIMING



Note: First gate line on timing



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7.4 Timing Parameters Table

MOD	3	resolution: 1920 (S) *1440 (G)					
SDCK[MHz]	40						
Pixels Per SDCK	8						
Line Parameters[SDCK]	LSL	LBL	LDL	LEL	GDCK_STA	LGONL	
	15	15	240	54	48	252	
Line Parameters[us]	/	/	/	/	/	/	
	0.38	0.38	6	1.35	1.2	6.3	
Frame Parameters[SDCK]	FSL	FBL	FDL	FEL	/	FR[Hz]	
	1	4	1440	10	/	84.85	
Frame Parameters[us]	/	/	/	/	/	/	
	8.10	32.40	11664.00	81.00	/	/	

Note:

1. For parameters definition, see EPD panel timing.
2. For Isis controller GDCK_STA and LGONL are not settable parameters; $GDCK_STA = LBL$, $LGONL = LDL + 0.5$
3. For Freescale SOC GDOE low pulse represent FSL and GDSP pulses with the first period of FBL.

7.5 Controller Timing

This timing mode is depicted on Figure 1 and Figure 2 and it refers to timing of Source Driver Output Enable (SDOE) and Gate Driver Clock (GDCK). Note, that in this mode LGON follows GDCK timing.

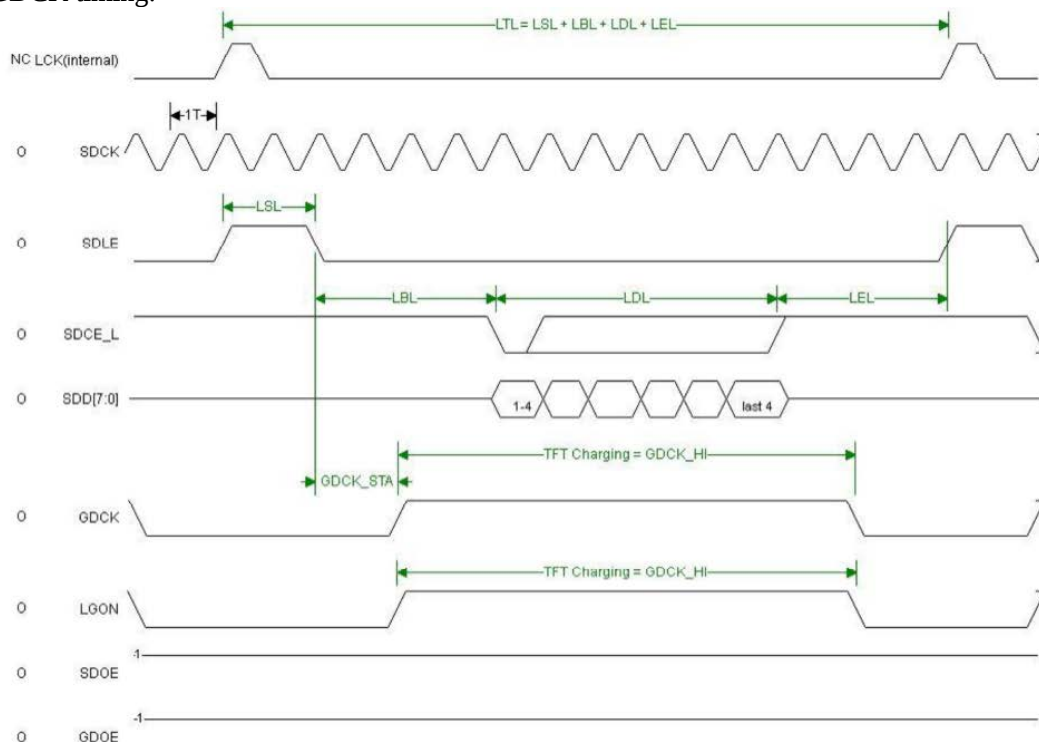


Figure 1. Line Timing in Mode 3

Note 1: LCK is an internal signal and it is shown for reference only.



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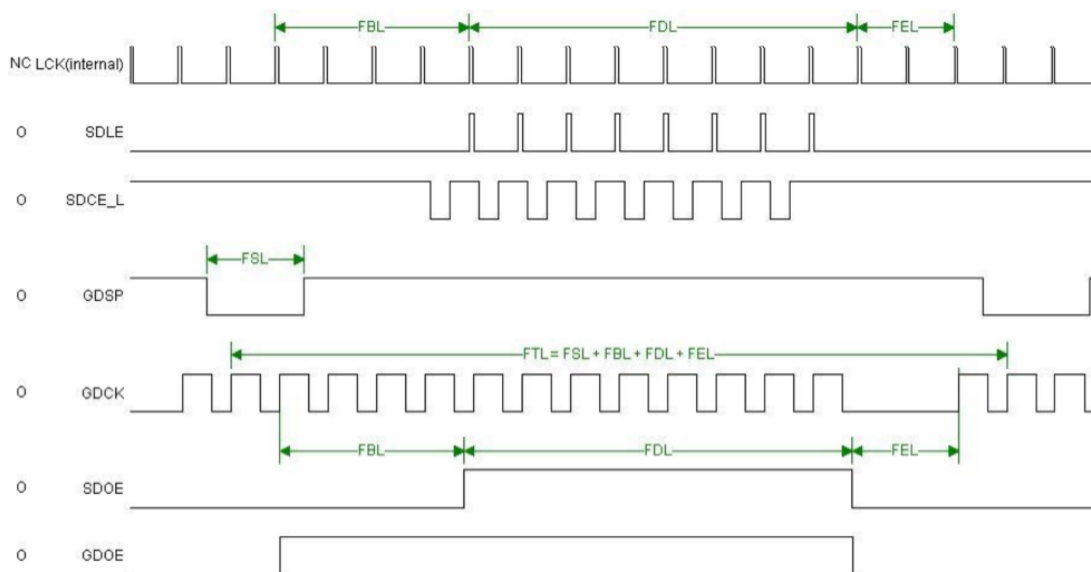


Figure 2 Frame Timing in Mode 3

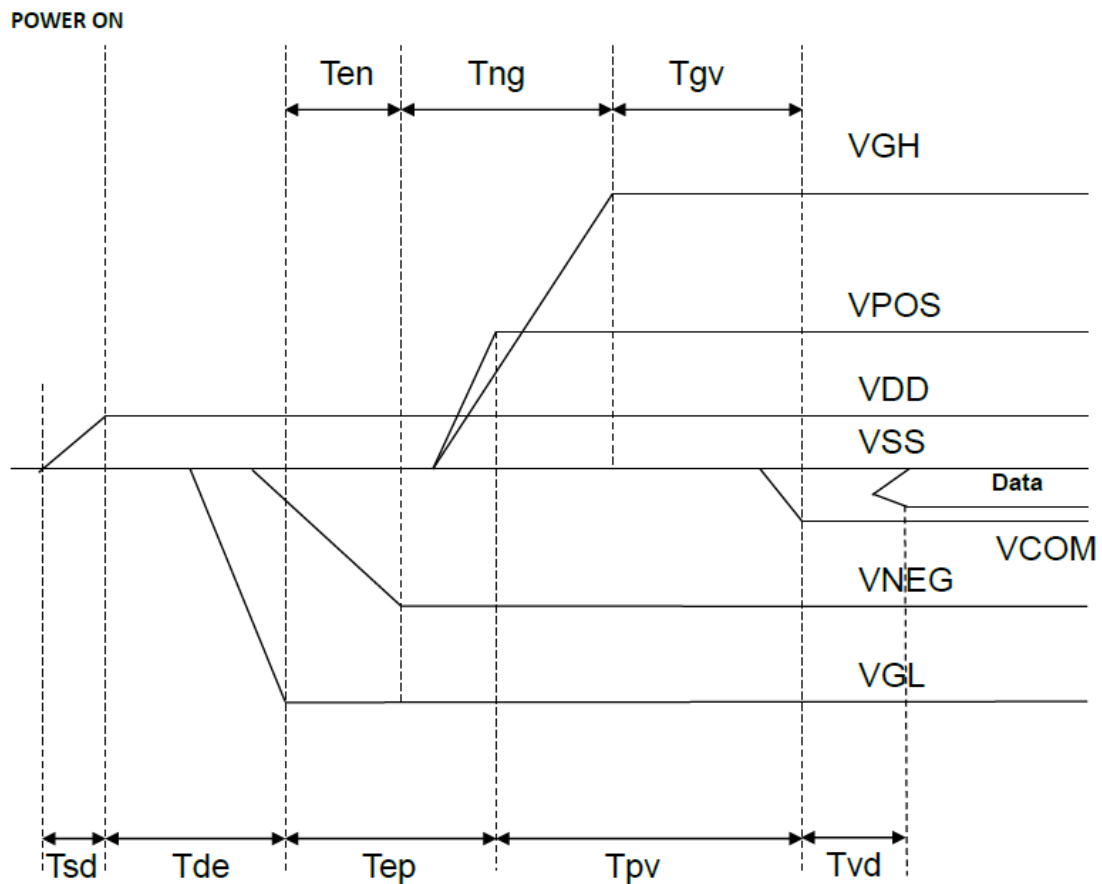


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8.Power Sequence

Power Rails must be sequenced in the following order:

1. VSS → VDD → VNEG → VPOS (Source driver) → VCOM
2. VSS → VDD → VGL → VGH (Gate driver)

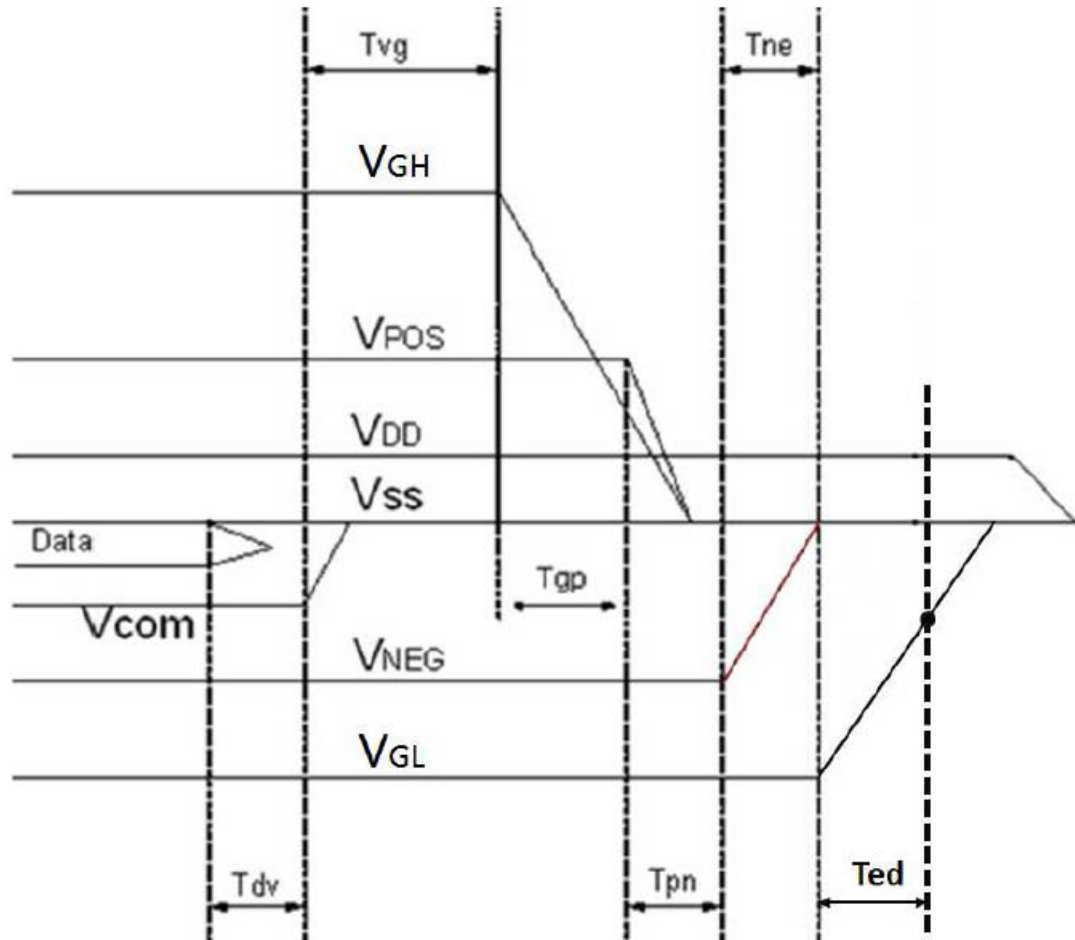


	Min	Max
Tsd	30us	-
Tde	100us	-
Tep	1000us	-
Tpv	100us	-
Tvd	100us	-
Ten	0us	-
Tng	1000us	-
Tgv	100us	-



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POWER OFF



	Min	Max	Remark
Tdv	100μs	-	-
Tvg	0μs	-	-
Tgp	0μs	-	-
Tpn	0μs	-	-
Tne	0μs	-	-
Ted	0.5s	-	Discharged point @ -7.4

Note 1 : Supply voltages decay through pull-down resistors.

Note 2 : Begin to turn off VGL power after VNEG and VPOS are completely or almost discharged to GND state.

Note 3 : VGL must remain negative of Vcom during decay period



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9. Optical characteristics

9.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

T = 25°C

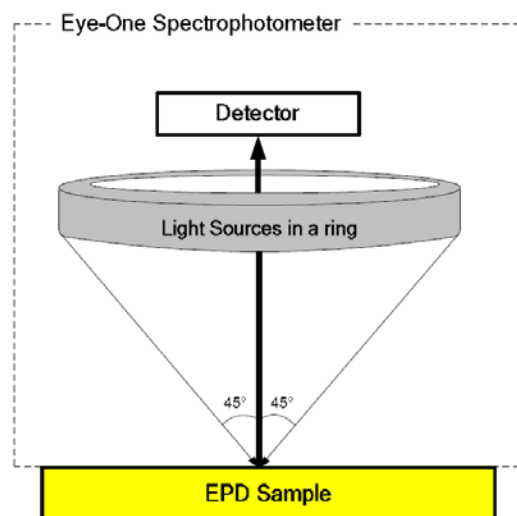
Symbol	Parameter	Conditions	Min	Typ.	Max	Unit	Note
R	Reflectance	White	35	40	-	%	Note 9-1
Gn	Nth Grey Level	-	-	$DS + (WS - DS) \times n / (m - 1)$	-	L*	-
CR	Contrast Ratio	-	13	18	-		-

WS: White state, DS: Dark state, Gray state from Dark to White :DS、G1、G2...、Gn...、Gm-2、WS m:4、8、16 when 2、3、4 bits mode

Note 9-1: Luminance meter :i- One Pro Spectrophotometer.

9.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd): $CR = Rl / Rd$



9.3 Reflection Ratio

The reflection ratio is expressed as:

$$R = \text{Reflectance Factor white board} \times (L_{\text{center}} / L_{\text{white board}})$$

Lcenter is the luminance measured at center in a white area (R=G=B=1). Lwhite board is the luminance of a standard white board. Both are measured with equivalent illumination source.

The viewing angle shall be no more than 2 degrees.



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10.Handling, Safety and Environmental Requirements and Remark

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION	
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.	
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.	
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.	
Mounting Precautions	
(1) It's recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.	
(2) It's recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.	
(3) You should adopt radiation structure to satisfy the temperature specification.	
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.	
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)	
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.	
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.	
Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
Remark	
All the specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any post-assembly operation.	



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11. Reliability test

	TEST	CONDITION	REMARK
1	High-Temperature Operation	T = +50°C, RH = 30% for 240 hrs	--
2	Low-Temperature Operation	T = 0°C for 240 hrs	--
3	High-Temperature Storage	T = +70°C, RH = 40% for 240 hrs, Test in white pattern	
4	Low-Temperature Storage	T = -25°C for 240 hrs, Test in white pattern	
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	--
6	High-Temperature, High-Humidity Storage	T = +60°C, RH = 80% for 240 hrs, Test in white pattern	
7	Temperature Cycle	-25°C (30min) ~ +70°C (30min), 100 Cycles, Test in white pattern	--
8	Solar radiation test	765 W/m ² for 168hrs, 40°C Test in white pattern	--
9	Electrostatic Effect (non-operating)	(Machine model) +/- 250V 0Ω, 200pF	--

Actual EMC level to be measured on customer application

Note: The protective film must be removed before temperature test.

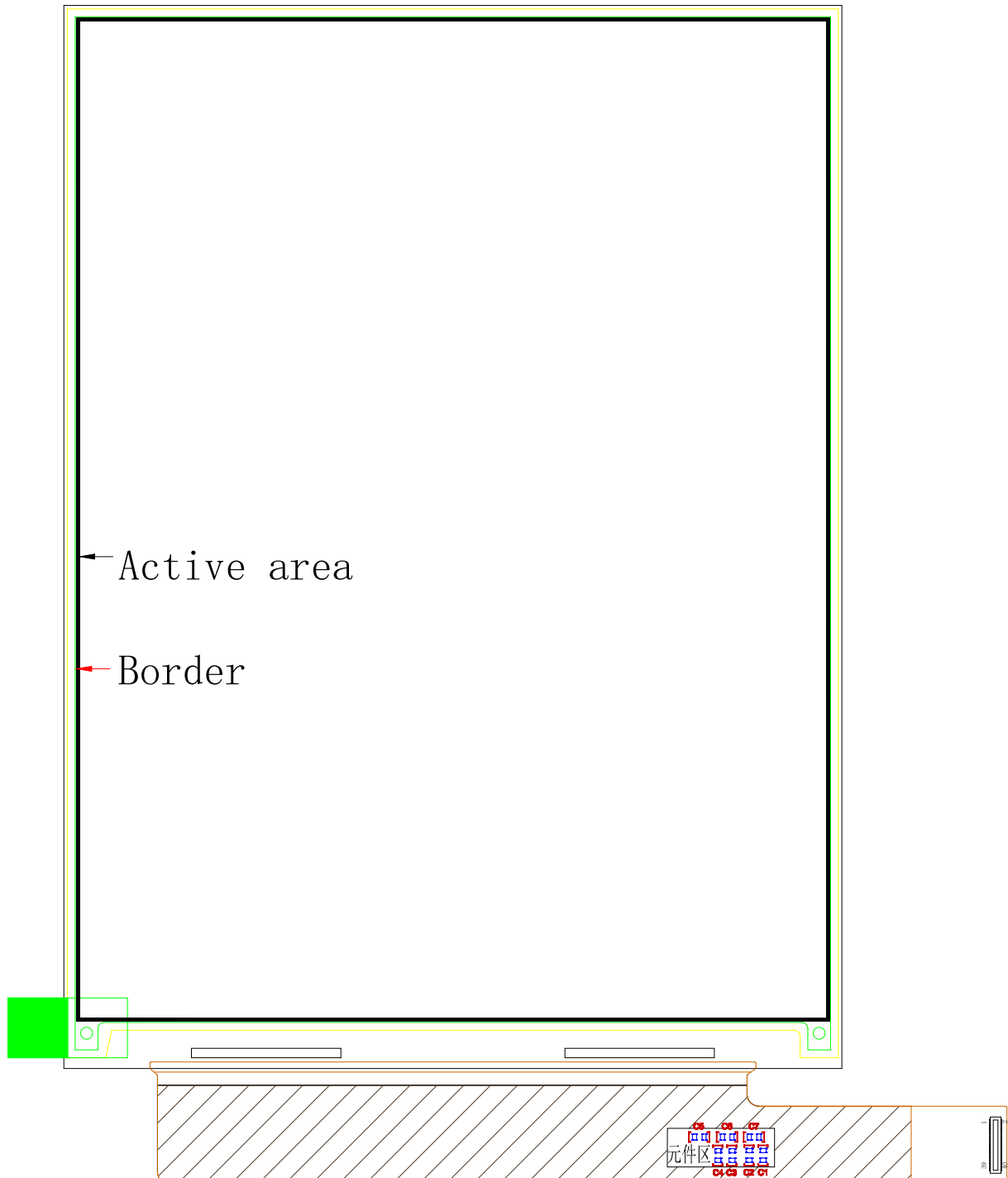
< Criteria >

In the standard conditions, there is not display function NG issue occurred. (including : line defect ,no image). All the cosmetic specification is judged before the reliability stress.



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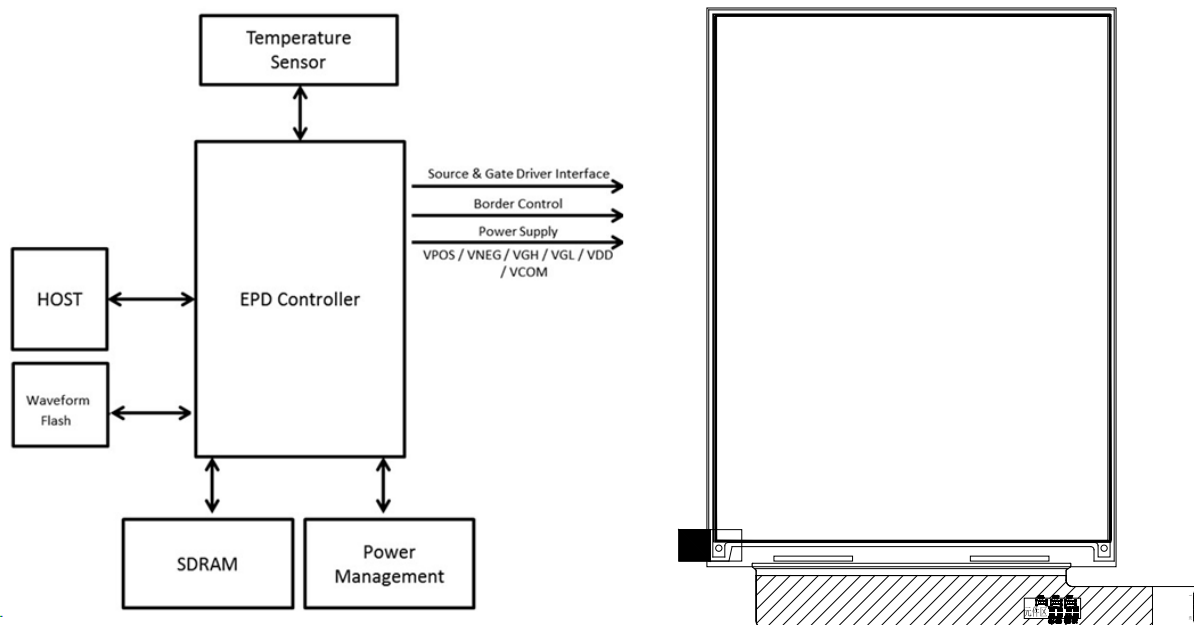
12.Border Definition





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13. Block Diagram





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14. Packing

The carton box size is 515*322*170mm.

