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Specification For HINK 3.7"EPD

Model NO: HINK-E037A30

Product VER:A0

Customer Approval

Customer	
Approval By	
Date Of Approval	

It will be agreed by the receiver,if not sign back the Specification within 15days.

Prepared By	Checked By	Approval By
Daisy Zhu	Zhou Yufeng	Hu Ziping



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Version	Content	Date	Producer
A0	New release	2022/03/31	Daisy Zhu



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1. General Description

HINK-E037A30 is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 3.7" active area contains 240×416 pixels, and has 1-bit B/W full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

2. Features

- 240×416 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Low voltage detect for supply voltage
- High voltage ready detect for driving voltage
- Internal temperature sensor
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor/ built-in temperature sensor

3. Application

Electronic Shelf Label System

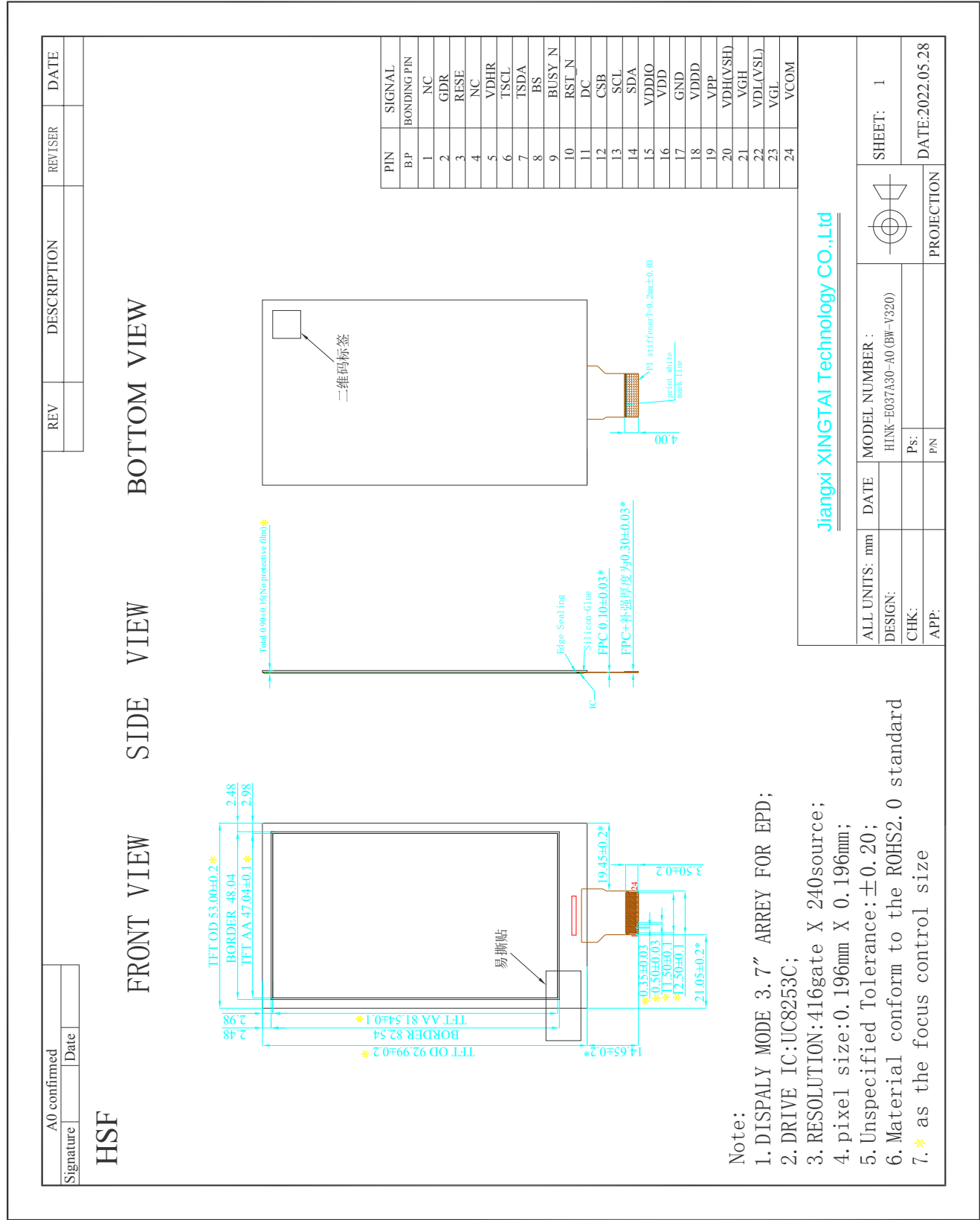
4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	3.7	Inch	
Display Resolution	240(H)×416(V)	Pixel	Dpi:130
Active Area	47.04(H)×81.54(V)	mm	
Pixel Pitch	0.196×0.196	mm	
Pixel Configuration	Rectangle		
Outline Dimension	53(H)×92.99 (V) ×0.90(D)	mm	Without masking film
Weight	8.5±0.5	g	



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5. Mechanical Drawing of EPD module





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6. Input/Output Terminals

Pin #	Single	Description	Remark
1	NC	No connection and do not connect with other NC pins	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins	Keep Open
5	VDHR	Positive Source driving voltage	
6	TSCL	I2C Interface to digital temperature sensor Clock pin	Note 6-6
7	TSDA	I2C Interface to digital temperature sensor Date pin	Note 6-6
8	BS	Bus selection pin	Note 6-5
9	BUSY_N	Busy state output pin	Note 6-4
10	RST_N	Reset	Note 6-3
11	DC	Data /Command control pin	Note 6-2
12	CSB	Chip Select input pin	Note 6-1
13	SCL	serial clock pin (SPI)	
14	SDA	serial data pin (SPI)	
15	VDDIO	Power for interface logic pins	
16	VDD	Power Supply pin for the chip	
17	GND	Ground	
18	VDDD	Core logic power pin	
19	VPP	Power Supply for OTP Programming	
20	VSH	Positive source driver Voltage	
21	VGH	Positive Gate driving voltage	
22	VSL	Negative Source driving voltage	
23	VGL	Negative Gate voltage.	
24	VCOM	VCOM driving voltage	

Note 6-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CSB is pulled LOW.

Note 6-2: This pin (DC) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 6-3: This pin (RST_N) is reset signal input. The Reset is active low.

Note 6-4: This pin (BUSY_N) is Driver busy flag.

L: Driver is Busy.

H: Host side can send command/data to driver.

Note 6-5: This pin (BS) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI is selected.

Note 6-6: If customer don't want to use external temperature sensors, please make TSCL and TSDA to be ground, not NC.



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7. Host interfaces

HT0001 provides 3-wire/4-wire serial interface for command and display data transferred from the MCU. The serial interface supports 8-bit mode. Data can be input/output by clocks while the chip is active (CSB =LOW). While input, data are written in order from MSB at the clock rising edge. When too many parameters are input, the chip accepts only defined parameters, and ignores undefined ones.

BS	Interface	CSB	DC	SCL	SDA
High	3-wire SPI	Available	Fix to GND	Available	Available
Low	4-wire SPI	Available	Available	Available	Available

3 wire SPI format

Data / Command is recognized with the first bit transferred. Data are transferred in the unit of 9 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 9 bits. (The serial counter is reset at the rising edge of the CSB signal.)

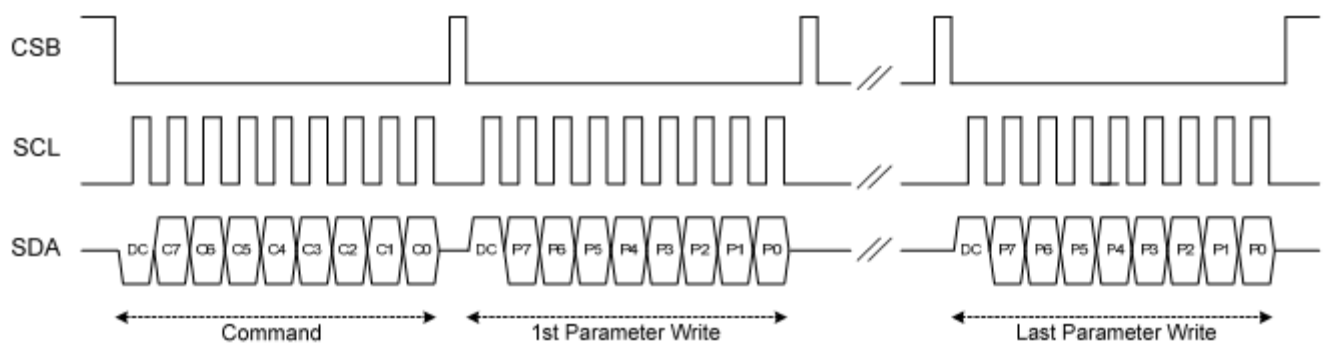


Figure: 3-wire SPI write operation

The MSB bit of data will be output at SDA pin after the 1st SCL falling edge, if the 1st input data at SDA is high.

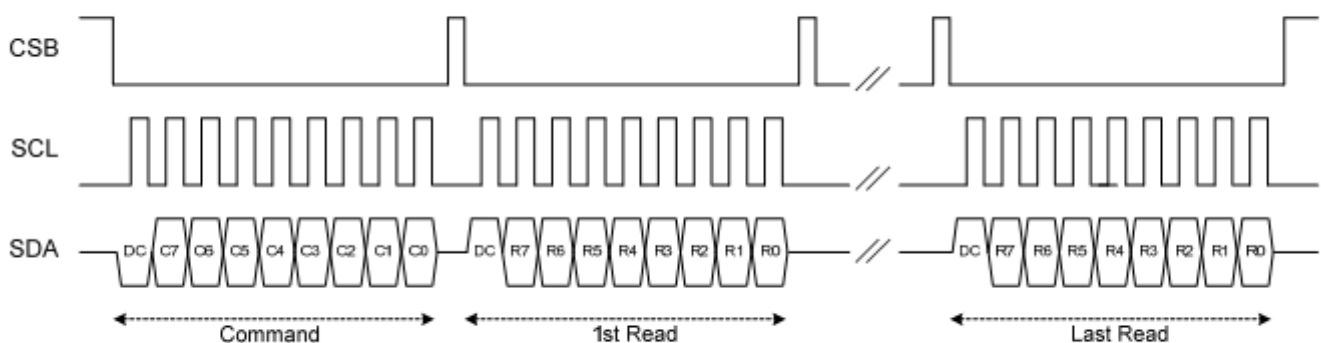


Figure: 3-wire SPI read operation



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4 wire SPI format

Data / Command is recognized with DC pin. Data are transferred in the unit of 8 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 8 bits. (The serial counter is reset at the rising edge of the CSB signal.)

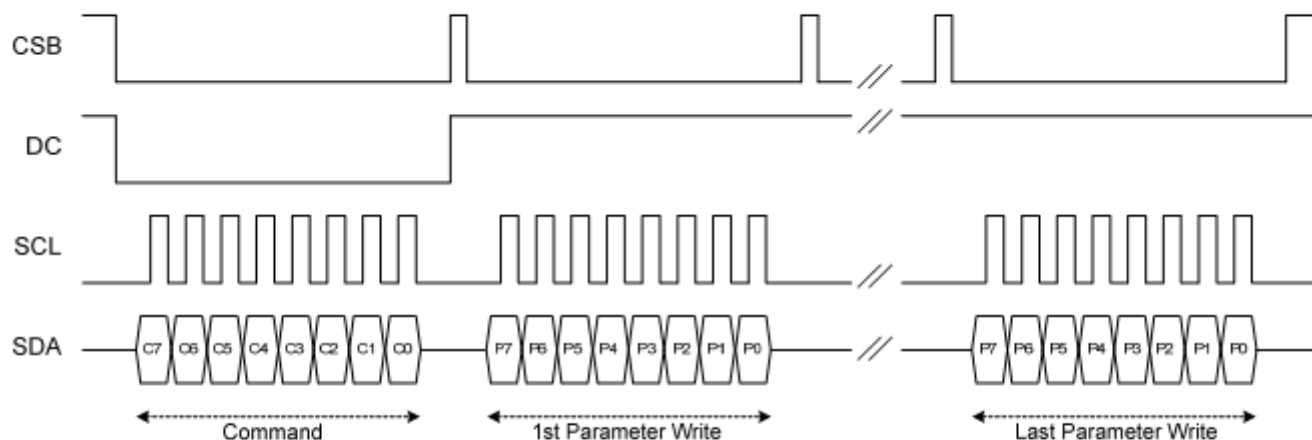


Figure: 4-wire SPI write operation

The MSB bit of data will be output at SDA pin after the CSB falling edge, if DC pin is High.

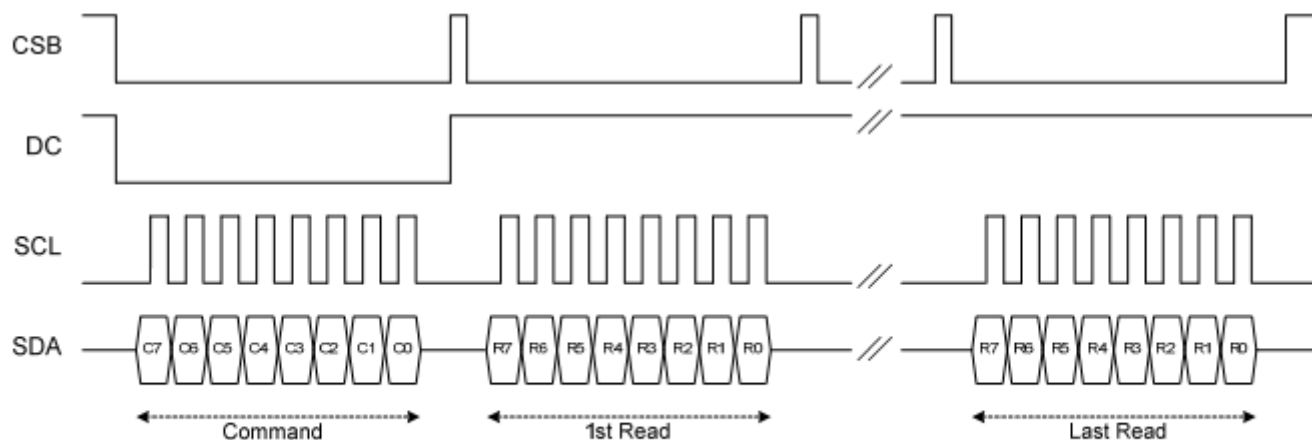


Figure: 4-wire SPI read operation



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8. Temperature sensor operation

Following is the way of how to sense the ambient temperature of the module. First, use an external temperature sensor to get the temperature value and converted it into HEX format with below mapping table, then send command 0x1A with the HEX temperature value to the module thru the SPI interface.

The temperature value to HEX conversion is as follow:

1. If the Temperature value MSByte bit D11 = 0, then

The temperature is positive and value (DegC) = + (Temperature value) / 16

2. If the Temperature value MSByte bit D11 = 1, then

The temperature is negative and value (DegC) = ~ (2's complement of Temperature value) / 16

12-bit binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
0111 1111 0000	7F0	2032	127
0111 1110 1110	7EE	2030	126.875
0111 1110 0010	7E2	2018	126.125
0111 1101 0000	7D0	2000	125
0001 1001 0000	190	400	25
0000 0000 0010	002	2	0.125
0000 0000 0000	000	0	0
1111 1111 1110	FFE	-2	-0.125
1110 0111 0000	E70	-400	-25
1100 1001 0010	C92	-878	-54.875
1100 1001 0000	C90	-880	-55



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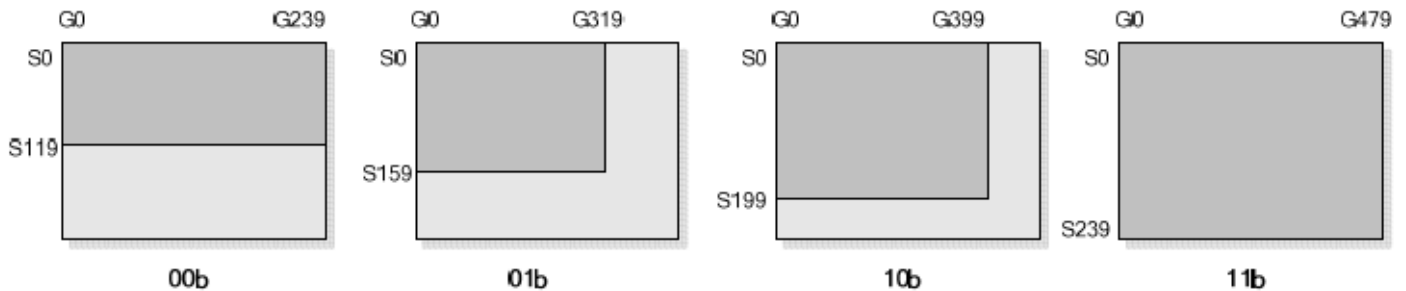
9. COMMAND TABLE

W/R: 0: Write Cycle / 1: Read Cycle **C/D**: 0: Command / 1: Data **D7-D0**: -: Don't Care

(1) PANEL SETTING (PSR) (REGISTER: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting the panel	0	0	0	0	0	0	0	0	0	0	00H
	0	1	RES1	RES0	REG	KW/R	UD	SHL	SHD_N	RST_N	0FH
	0	1	0	0	0	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	0DH

RES[1:0]: Display Resolution setting (source x gate)
00b: 240x120 (Default) Active gate channels: G0 ~ G239. Active source channels: S0 ~ S119.
01b: 320x160 Active gate channels: G0 ~ G319. Active source channels: S0 ~ S159.
10b: 400x200 Active gate channels: G0 ~ G399. Active source channels: S0 ~ S199.
11b: 480x240 Active gate channels: G0 ~ G479. Active source channels: S0 ~ S239.



REG: LUT selection

0: LUT from OTP. (Default)
1: LUT from register.

KW/R: Black / White / Red

0: Pixel with Black/White/Red, KWR mode. (Default)
1: Pixel with Black/White, KW mode.

UD: Gate Scan Direction

0: Scan down. First line to Last line: Gn-1 → Gn-2 → Gn-3 → ... → G0
1: Scan up. (Default) First line to Last line: G0 → G1 → G2 → ... → Gn-1

SHL: Source Shift Direction

0: Shift left. First data to Last data: Sn-1 → Sn-2 → Sn-3 → ... → S0
1: Shift right. (Default) First data to Last data: S0 → S1 → S2 → ... → Sn-1

SHD_N: Booster Switch

0: Booster OFF
1: Booster ON (Default)

When SHD_N becomes LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF. And Source/Gate/Border/VCOM will be released to floating.

RST_N: Soft Reset

0: Reset. Booster OFF, Register data are set to their default values, all drivers will be reset, and all functions will be disabled. Source/Gate/Border/VCOM will be released to floating. After soft reset is transmitted, the internal operation needs at least 50uS to execute. During this period of time, the BUSY_N pin keeps low and any command will be ignored.

1: No effect (Default).



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VCMZ: VCOM Hi-Z state function

0: No effect (Default)

1 : VCOM is always floating

TS_AUTO: Temperature sensor will be activated automatically one time.

0: No effect

1: Before enabling booster, Temperature Sensor will be activated automatically one time (Default).

TIEG: VGL state function

0: No effect

1 : After power off booster, VGL will be tied to GND (Default).

NORG: VCOM state during refreshing display

0: No effect (Default)

1: Expect refreshing display, VCOM is tied to GND.

VC_LUTZ: VCOM state during refreshing display

0: No effect

1: After refreshing display, the output of VCOM is set to floating automatically (Default).

Note: Priority of Vcom setting: VCMZ > EOPT > NORG > VC_LUTZ



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(2) POWER SETTING (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1	01H
	0	1	-	-	-	BD_EN	-	-	VDS_EN	VDG_EN	03H
	0	1	-	-	-	VCOM_SLEW	VGHL_LV[3:0]				10H
	0	1	-	-	VSH[5:0]						3FH
	0	1	-	-	VSL[5:0]						3FH
	0	1	OPTEN	VDHR[6:0]							0DH

BD_EN: Border LDO enable
0 : Border LDO disable (Default)
 Border level selection: 00b: VCOM 01b: VDH 10b: VDL 11b: VDHR
1 : Border LDO enable
 Border level selection: 00b: VCOM 01b: VBH(VCOM-VDL) 10b: VBL(VCOM-VDH) 11b: VDHR

VDS_EN: Source power selection
0 : External source power from VSH/VSL/VDHR pins
1 : Internal DC/DC function for generating VSH/VSL/VDHR. (Default)

VDG_EN: Gate power selection
0 : External gate power from VGH/VGL pins
1 : Internal DC/DC function for generating VGH/VGL. (Default)

VCOM_SLEW: VCOM slew rate selection for voltage transition. The value is fixed at 1.

VGHL_LV[3:0]: VGH / VGL Voltage Level selection.

VGHL_LV	VGHL Voltage Level
0000 (Default)	VGH=20V, VGL= -20V
0001	VGH=19V, VGL= -19V
0010	VGH=18V, VGL= -18V
0011	VGH=17V, VGL= -17V
0100	VGH=16V, VGL= -16V
0101	VGH=15V, VGL= -15V
0110	VGH=14V, VGL= -14V
0111	VGH=13V, VGL= -13V
1000	VGH=12V, VGL= -12V
1001	VGH=11V, VGL= -11V
1010	VGH=10V, VGL= -10V

VSH[5:0]: Internal VSH power selection for B/W pixel. (Default value: 11 1111b)

VSH	Voltage	VSH	Voltage	VSH	Voltage	VSH	Voltage
00 0000	2.4 V	01 0000	5.6 V	10 0000	8.8 V	11 0000	12.0 V
00 0001	2.6 V	01 0001	5.8 V	10 0001	9.0 V	11 0001	12.2 V
00 0010	2.8 V	01 0010	6.0 V	10 0010	9.2 V	11 0010	12.4 V
00 0011	3.0 V	01 0011	6.2 V	10 0011	9.4 V	11 0011	12.6 V
00 0100	3.2 V	01 0100	6.4 V	10 0100	9.6 V	11 0100	12.8 V
00 0101	3.4 V	01 0101	6.6 V	10 0101	9.8 V	11 0101	13.0 V
00 0110	3.6 V	01 0110	6.8 V	10 0110	10.0V	11 0110	13.2 V
00 0111	3.8 V	01 0111	7.0 V	10 0111	10.2 V	11 0111	13.4 V
00 1000	4.0 V	01 1000	7.2 V	10 1000	10.4 V	11 1000	13.6 V
00 1001	4.2 V	01 1001	7.4 V	10 1001	10.6 V	11 1001	13.8 V
00 1010	4.4 V	01 1010	7.6 V	10 1010	10.8 V	11 1010	14.0 V
00 1011	4.6 V	01 1011	7.8 V	10 1011	11.0 V	11 1011	14.2 V
00 1100	4.8 V	01 1100	8.0 V	10 1100	11.2 V	11 1100	14.4 V
00 1101	5.0 V	01 1101	8.2V	10 1101	11.4 V	11 1101	14.6 V
00 1110	5.2 V	01 1110	8.4 V	10 1110	11.6 V	11 1110	14.8 V
00 1111	5.4 V	01 1111	8.6 V	10 1111	11.8 V	11 1111	15.0 V

VSL[5:0]: Internal VSL power selection for B/W pixel. (Default value: 11 1111b)



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VSL	Voltage	VSL	Voltage	VSL	Voltage	VSL	Voltage
00 0000	-2.4 V	01 0000	-5.6 V	10 0000	-8.8 V	11 0000	-12.0 V
00 0001	-2.6 V	01 0001	-5.8 V	10 0001	-9.0 V	11 0001	-12.2 V
00 0010	-2.8 V	01 0010	-6.0 V	10 0010	-9.2 V	11 0010	-12.4 V
00 0011	-3.0 V	01 0011	-6.2 V	10 0011	-9.4 V	11 0011	-12.6 V
00 0100	-3.2 V	01 0100	-6.4 V	10 0100	-9.6 V	11 0100	-12.8 V
00 0101	-3.4 V	01 0101	-6.6 V	10 0101	-9.8 V	11 0101	-13.0 V
00 0110	-3.6 V	01 0110	-6.8 V	10 0110	-10.0 V	11 0110	-13.2 V
00 0111	-3.8 V	01 0111	-7.0 V	10 0111	-10.2 V	11 0111	-13.4 V
00 1000	-4.0 V	01 1000	-7.2 V	10 1000	-10.4 V	11 1000	-13.6 V
00 1001	-4.2 V	01 1001	-7.4 V	10 1001	-10.6 V	11 1001	-13.8 V
00 1010	-4.4 V	01 1010	-7.6 V	10 1010	-10.8 V	11 1010	-14.0 V
00 1011	-4.6 V	01 1011	-7.8 V	10 1011	-11.0 V	11 1011	-14.2 V
00 1100	-4.8 V	01 1100	-8.0 V	10 1100	-11.2 V	11 1100	-14.4 V
00 1101	-5.0 V	01 1101	-8.2 V	10 1101	-11.4 V	11 1101	-14.6 V
00 1110	-5.2 V	01 1110	-8.4 V	10 1110	-11.6 V	11 1110	-14.8 V
00 1111	-5.4 V	01 1111	-8.6 V	10 1111	-11.8 V	11 1111	-15.0 V

VDHR[5:0]: Internal VDHR power selection for Red pixel. (Default value: 001101b)

VDHR	Voltage	VDHR	Voltage	VDHR	Voltage	VDHR	Voltage
00 0000	2.4 V	01 0000	5.6 V	10 0000	8.8 V	11 0000	12.0 V
00 0001	2.6 V	01 0001	5.8 V	10 0001	9.0 V	11 0001	12.2 V
00 0010	2.8 V	01 0010	6.0 V	10 0010	9.2 V	11 0010	12.4 V
00 0011	3.0 V	01 0011	6.2 V	10 0011	9.4 V	11 0011	12.6 V
00 0100	3.2 V	01 0100	6.4 V	10 0100	9.6 V	11 0100	12.8 V
00 0101	3.4 V	01 0101	6.6 V	10 0101	9.8 V	11 0101	13.0 V
00 0110	3.6 V	01 0110	6.8 V	10 0110	10.0 V	11 0110	13.2 V
00 0111	3.8 V	01 0111	7.0 V	10 0111	10.2 V	11 0111	13.4 V
00 1000	4.0 V	01 1000	7.2 V	10 1000	10.4 V	11 1000	13.6 V
00 1001	4.2 V	01 1001	7.4 V	10 1001	10.6 V	11 1001	13.8 V
00 1010	4.4 V	01 1010	7.6 V	10 1010	10.8 V	11 1010	14.0 V
00 1011	4.6 V	01 1011	7.8 V	10 1011	11.0 V	11 1011	14.2 V
00 1100	4.8 V	01 1100	8.0 V	10 1100	11.2 V	11 1100	14.4 V
00 1101	5.0 V	01 1101	8.2 V	10 1101	11.4 V	11 1101	14.6 V
00 1110	5.2 V	01 1110	8.4 V	10 1110	11.6 V	11 1110	14.8 V
00 1111	5.4 V	01 1111	8.6 V	10 1111	11.8 V	11 1111	15.0 V



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OPTEN: 1 enable step-0.1V voltage selection.

VDHR	Voltage	VDHR	Voltage	VDHR	Voltage	VDHR	Voltage
1000 0000	2.4 V	1010 0000	5.6 V	1100 0000	8.8 V	1110 0000	12 V
1000 0001	2.5 V	1010 0001	5.7 V	1100 0001	8.9 V	1110 0001	12.1 V
1000 0010	2.6 V	1010 0010	5.8 V	1100 0010	9.0 V	1110 0010	12.2 V
1000 0011	2.7 V	1010 0011	5.9 V	1100 0011	9.1 V	1110 0011	12.3 V
1000 0100	2.8 V	1010 0100	6.0 V	1100 0100	9.2 V	1110 0100	12.4 V
1000 0101	2.9 V	1010 0101	6.1 V	1100 0101	9.3 V	1110 0101	12.5 V
1000 0110	3.0 V	1010 0110	6.2 V	1100 0110	9.4 V	1110 0110	12.6 V
1000 0111	3.1 V	1010 0111	6.3 V	1100 0111	9.5 V	1110 0111	12.7 V
1000 1000	3.2 V	1010 1000	6.4 V	1100 1000	9.6 V	1110 1000	12.8 V
1000 1001	3.3 V	1010 1001	6.5 V	1100 1001	9.7 V	1110 1001	12.9 V
1000 1010	3.4 V	1010 1010	6.6 V	1100 1010	9.8 V	1110 1010	13.0 V
1000 1011	3.5 V	1010 1011	6.7 V	1100 1011	9.9 V	1110 1011	13.1 V
1000 1100	3.6 V	1010 1100	6.8 V	1100 1100	10.0 V	1110 1100	13.2 V
1000 1101	3.7 V	1010 1101	6.9 V	1100 1101	10.1 V	1110 1101	13.3 V
1000 1110	3.8 V	1010 1110	7.0 V	1100 1110	10.2 V	1110 1110	13.4 V
1000 1111	3.9 V	1010 1111	7.1 V	1100 1111	10.3 V	1110 1111	13.5 V
1001 0000	4.0 V	1011 0000	7.2 V	1101 0000	10.4 V	1111 0000	13.6 V
1001 0001	4.1 V	1011 0001	7.3 V	1101 0001	10.5 V	1111 0001	13.7 V
1001 0010	4.2 V	1011 0010	7.4 V	1101 0010	10.6 V	1111 0010	13.8 V
1001 0011	4.3 V	1011 0011	7.5 V	1101 0011	10.7 V	1111 0011	13.9 V
1001 0100	4.4 V	1011 0100	7.6 V	1101 0100	10.8 V	1111 0100	14.0 V
1001 0101	4.5 V	1011 0101	7.7 V	1101 0101	10.9 V	1111 0101	14.1 V
1001 0110	4.6 V	1011 0110	7.8 V	1101 0110	11.0 V	1111 0110	14.2 V
1001 0111	4.7 V	1011 0111	7.9 V	1101 0111	11.1 V	1111 0111	14.3 V
1001 1000	4.8 V	1011 1000	8.0 V	1101 1000	11.2 V	1111 1000	14.4 V
1001 1001	4.9 V	1011 1001	8.1 V	1101 1001	11.3 V	1111 1001	14.5 V
1001 1010	5.0 V	1011 1010	8.2 V	1101 1010	11.4 V	1111 1010	14.6 V
1001 1011	5.1 V	1011 1011	8.3 V	1101 1011	11.5 V	1111 1011	14.7 V
1001 1100	5.2 V	1011 1100	8.4 V	1101 1100	11.6 V	1111 1100	14.8 V
1001 1101	5.3 V	1011 1101	8.5 V	1101 1101	11.7 V	1111 1101	14.9 V
1001 1110	5.4 V	1011 1110	8.6 V	1101 1110	11.8 V	1111 1110	15.0 V
1001 1111	5.5 V	1011 1111	8.7 V	1101 1111	11.9 V		

(3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	0	0	0	0	0	0	0	0	1	0

After the Power OFF command, the driver will be powered OFF. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode. Source/Gate/Border/VCOM will be released to floating.

(4) POWER OFF SEQUENCE SETTING (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1
	0	1	-	-	T_VDS_OFF[1:0]	-	-	-	-	-

T_VDS_OFF[1:0]: Source to gate power off interval time.

00b: 1 frame (Default)

01b: 2 frames

10b: 3 frames

11b: 4 frame



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(5) POWER ON (PON) (REGISTER: R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the power	0	0	0	0	0	0	0	1	0	0

After the Power ON command, the driver will be powered ON. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUSY_N signal will return to high.

(6) BOOSTER SOFT START (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	0	0	1	1	0
	0	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0
	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0

BTPHA[7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA[5:3]: Driving strength of phase A

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHA[2:0]: Minimum OFF time setting of GDR in phase A

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHB[7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHB[5:3]: Driving strength of phase B

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHB[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHC[5:3]: Driving strength of phase C

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHC[2:0]: Minimum OFF time setting of GDR in phase C

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**



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(7) DEEP SLEEP (DSLP) (R07h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Deep Sleep	0	0	0	0	0	0	0	1	1	1	07h
	0	1	1	0	1	0	0	1	0	1	A5h

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

(8) DATA START TRANSMISSION 1 (DTM1) (R10h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	0	0	10h
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	00h
	0	1	:	:	:	:	:	:	:	:	00h
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	00h

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes "OLD" data to SRAM.

In KWR mode, this command writes "B/W" data to SRAM.

In Program mode, this command writes "OTP" data to SRAM for programming.

(9) DATA STOP (DSP) (R11h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	0	0	0	1	0	0	0	1	11h
	1	1	data_flag	-	-	-	-	-	-	-	00h

Check the completeness of data. If data is complete, start to refresh display.

Data_flag: Data flag of receiving user data.

0: Driver didn't receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After "Data Start" (R10h) or "Data Stop" (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY_N signal will become "0".

(10) DISPLAY REFRESH (DRF) (R12h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Refreshing the display	0	0	0	0	0	1	0	0	1	0	12h

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY_N signal will become "0" and the refreshing of panel starts.

The waiting interval from BUSY_N falling to the first FLG command must be larger than 200uS.

(11) DATA START TRANSMISSION 2 (DTM2) (R13h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	1	1	13h
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	00h
	0	1	:	:	:	:	:	:	:	:	00h
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	00h

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes "NEW" data to SRAM.

In KWR mode, this command writes "RED" data to SRAM.



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(12) PLL CONTROL (PLL) (R30H)

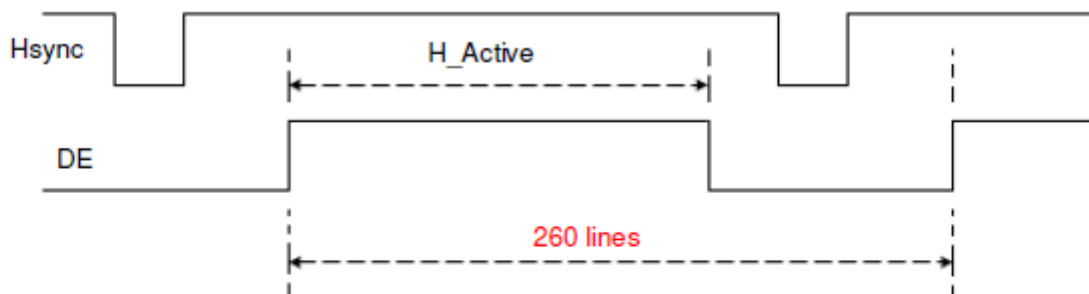
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Controlling PLL	0	0	0	0	1	1	0	0	0	0
	0	1	-	-	-	FRS[4:0]				

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

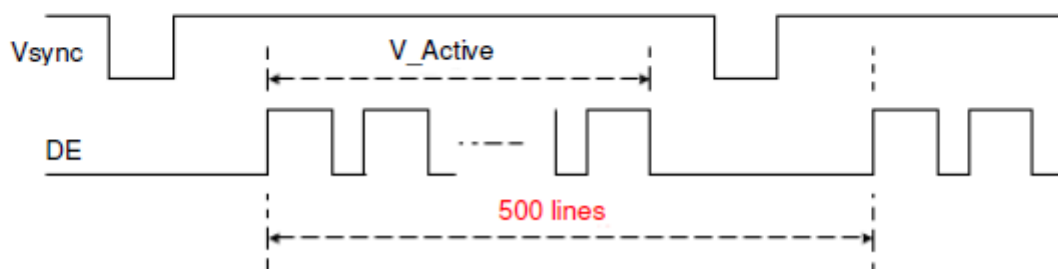
FMR[4:0]: Frame rate setting

FRS	Frame rate	FRS	Frame rate
00000	5Hz	10000	85Hz
00001	10Hz	10001	90Hz
00010	15Hz	10010	95Hz
00011	20Hz	10011	100Hz
00100	25Hz	10100	105Hz
00101	30Hz	10101	110Hz
00110	35Hz	10110	115Hz
00111	40Hz	10111	120Hz
01000	45Hz	11000	130Hz
01001	50Hz	11001	140Hz
01010	55Hz	11010	150Hz
01011	60Hz	11011	160Hz
01100	65Hz	11100	170Hz
01101	70Hz	11101	180Hz
01110	75Hz	11110	190Hz
01111	80Hz	11111	200Hz

Horizontal



Vertical





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(13) VCOM AND DATA INTERVAL SETTING (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval between VCOM and Data	0	0	0	1	0	1	0	0	0	0
	0	1	VBD[1:0]		DDX[1:0]		CDI[3:0]			

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

VBD[1:0]: Border data selection

KWR mode (KW/R=0)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTK
1 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	Floating

KW mode (KW/R=1)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	Floating
1 (Default)	00	Floating
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	Floating

DDX[1:0]: Data polarity.

Under KWR mode (KW/R=0):

DDX[1] is for RED data.

DDX[0] is for B/W data.

DDX[1:0]	Data (Red, B/W)	LUT
00	00	LUTW
	01	LUTK
	10	LUTR
	11	LUTR
01 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTR

DDX[1:0]	Data (Red, B/W)	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTK
11	00	LUTR
	01	LUTR
	10	LUTK
	11	LUTW

Under KW mode (KW/R=1):

DDX[1]=0 is for KW mode with NEW/OLD,

DDX[1]=1 is for KW mode without NEW/OLD.

DDX[1:0]	Data (NEW, OLD)	LUT
00	00	LUTWW (0 → 0)
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (1 → 1)
01 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTWW (1 → 1)

DDX[1:0]	Data (NEW)	LUT
10	0	LUTKW (1 → 0)
	1	LUTWK (0 → 1)
11	0	LUTWK (1 → 0)
	1	LUTKW (0 → 1)



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(14) RESOLUTION SETTING (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	0	1	1	0	0	0	0	1	61h
	0	1	HRES[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	VRES[8]	00h
	0	1	VRES[7:0]								00h

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[7:3]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Active channel calculation, assuming HRES[7:3]=0, VRES[8:0]=0:

Gate: First active gate = G0;
Last active gate = VRES[8:0] - 1

Source: First active source = S0;
Last active source = HRES[7:3]*8 - 1

Example: 128 (source) x 272 (gate), assuming HRES[7:3]=0, VRES[8:0]=0

Gate: First active gate = G0,
Last active gate = G271; (VRES[8:0] = 272, 272 - 1 = 271)

Source: First active source = S0,
Last active source = S127; (HRES[7:3]=16, 16*8 - 1 = 127)

(15) GATE/SOURCE START SETTING (GSST) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Start	0	0	0	1	1	0	0	1	0	1	65h
	0	1	HST[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	VST[8]	00h
	0	1	VST[7:0]								00h

This command defines resolution start gate/source position.

HST[7:3]: Horizontal Display Start Position (Source)

VST[8:0]: Vertical Display Start Position (Gate)

Example : For 128(Source) x 240(Gate)

HST[7:3] = 4 (HST[8:0] = 4*8 = 32),
VST[8:0] = 32

Gate: First active gate = G32 (VST[8:0] = 32),
Last active gate = G271 (VST[8:0] = 32, VRES[8:0] = 240, 32+240-1=271)

Source: First active source = S32 (HST[7:3] = 32),
Last active source = S159 (HST[7:3] = 32, HRES[8:0] = 128, 32+128-1=159)



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(16) VCOM_DC SETTING (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set VCOM_DC	0	0	1	0	0	0	0	0	1	0	82h
	0	1	-	-	VDCS[6:0]						00h

This command sets VCOM_DC value

VDCS[6:0]: VCOM_DC Setting

VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)
0000000b	-0.1	0101011b	-4.4	1010110b	-8.7
0000001b	-0.2	0101100b	-4.5	1010111b	-8.8
0000010b	-0.3	0101101b	-4.6	1011000b	-8.9
0000011b	-0.4	0101110b	-4.7	1011001b	-9
0000100b	-0.5	0101111b	-4.8	1011010b	-9.1
0000101b	-0.6	0110000b	-4.9	1011011b	-9.2
0000110b	-0.7	0110001b	-5	1011100b	-9.3
0000111b	-0.8	0110010b	-5.1	1011101b	-9.4
0001000b	-0.9	0110011b	-5.2	1011110b	-9.5
0001001b	-1	0110100b	-5.3	1011111b	-9.6
0001010b	-1.1	0110101b	-5.4	1100000b	-9.7
0001011b	-1.2	0110110b	-5.5	1100001b	-9.8
0001100b	-1.3	0110111b	-5.6	1100010b	-9.9
0001101b	-1.4	0111000b	-5.7	1100011b	-10
0001110b	-1.5	0111001b	-5.8	1100100b	-10.1
0001111b	-1.6	0111010b	-5.9	1100101b	-10.2
0010000b	-1.7	0111011b	-6	1100110b	-10.3
0010001b	-1.8	0111100b	-6.1	1100111b	-10.4
0010010b	-1.9	0111101b	-6.2	1101000b	-10.5
0010011b	-2	0111110b	-6.3	1101001b	-10.6
0010100b	-2.1	0111111b	-6.4	1101010b	-10.7
0010101b	-2.2	1000000b	-6.5	1101011b	-10.8
0010110b	-2.3	1000001b	-6.6	1101100b	-10.9
0010111b	-2.4	1000010b	-6.7	1101101b	-11
0011000b	-2.5	1000011b	-6.8	1101110b	-11.1
0011001b	-2.6	1000100b	-6.9	1101111b	-11.2
0011010b	-2.7	1000101b	-7	1110000b	-11.3
0011011b	-2.8	1000110b	-7.1	1110001b	-11.4
0011100b	-2.9	1000111b	-7.2	1110010b	-11.5
0011101b	-3	1001000b	-7.3	1110011b	-11.6
0011110b	-3.1	1001001b	-7.4	1110100b	-11.7
0011111b	-3.2	1001010b	-7.5	1110101b	-11.8
0100000b	-3.3	1001011b	-7.6	1110110b	-11.9
0100001b	-3.4	1001100b	-7.7	1110111b	-12
0100010b	-3.5	1001101b	-7.8	1111000b	-12.1
0100011b	-3.6	1001110b	-7.9	1111001b	-12.2
0100100b	-3.7	1001111b	-8	1111010b	-12.3
0100101b	-3.8	1010000b	-8.1	1111011b	-12.4
0100110b	-3.9	1010001b	-8.2	1111100b	-12.5
0100111b	-4	1010010b	-8.3	1111101b	-12.6
0101000b	-4.1	1010011b	-8.4	1111110b	-12.7
0101001b	-4.2	1010100b	-8.5		
0101010b	-4.3	1010101b	-8.6		



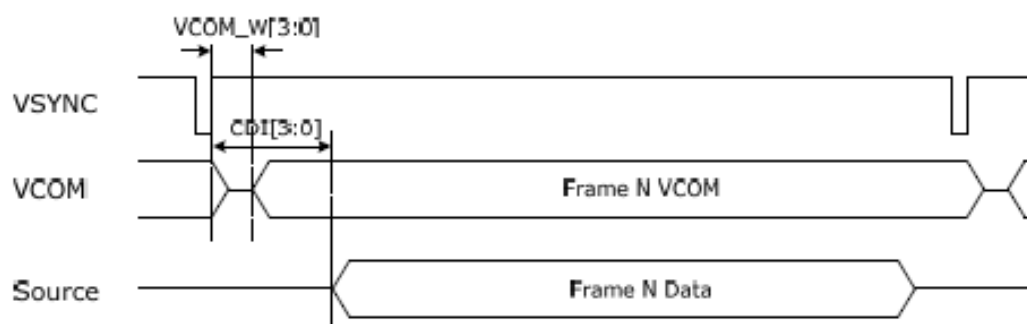
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(17) POWER SAVING (PWS) (RE3H)

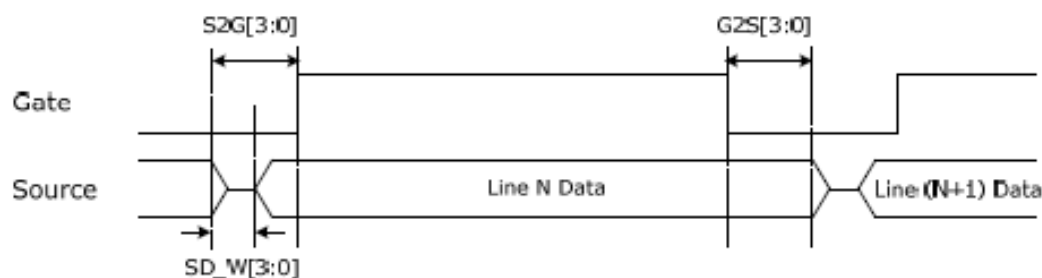
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power Saving for VCOM & Source	0	0	1	1	1	0	0	0	1	1	E3h
	0	1	VCOM_W[3:0]				SD_W[3:0]				00h

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (unit = line period)



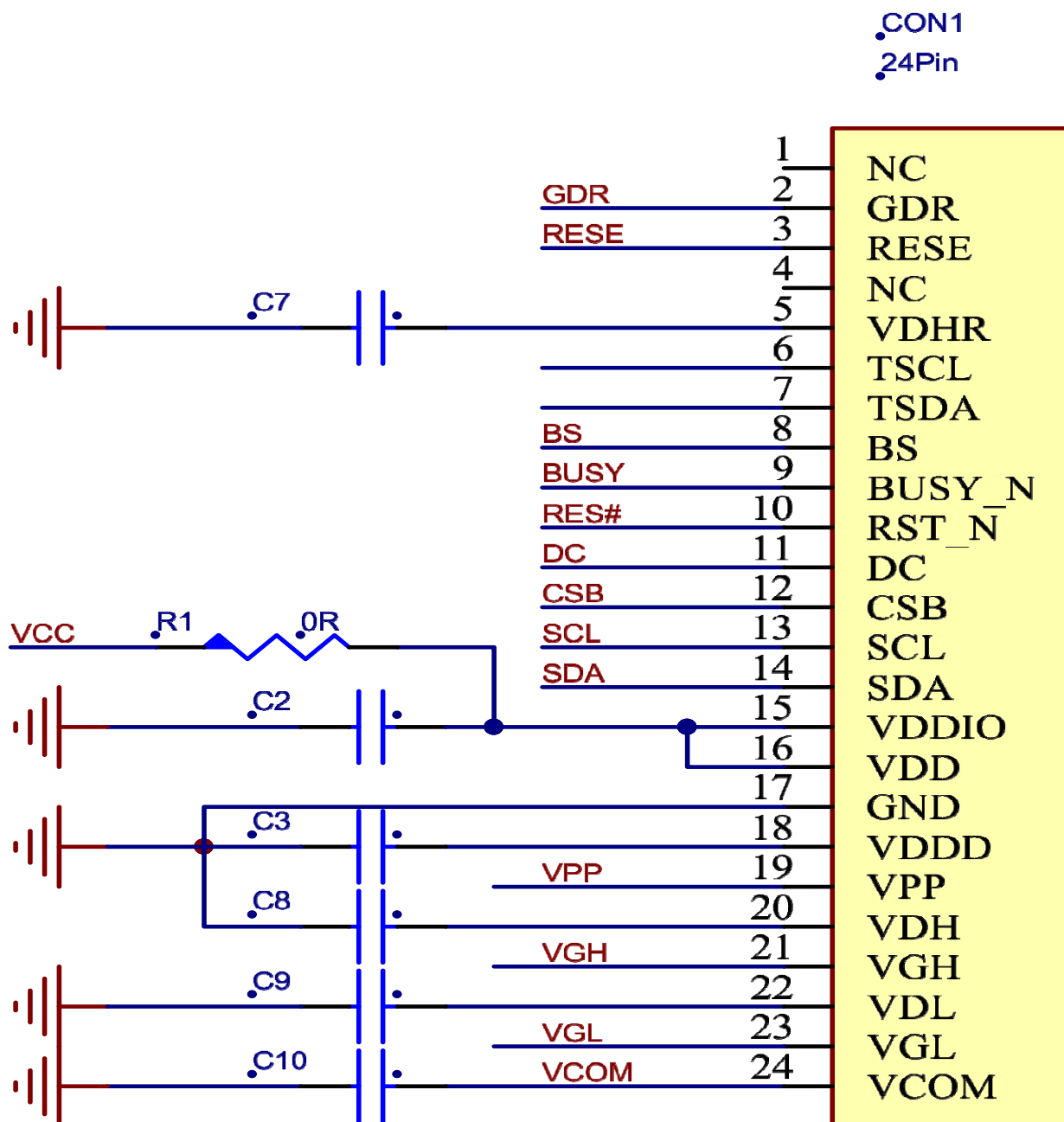
SD_W[3:0]: Source power saving width (unit = 650nS)





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10. Reference Circuit





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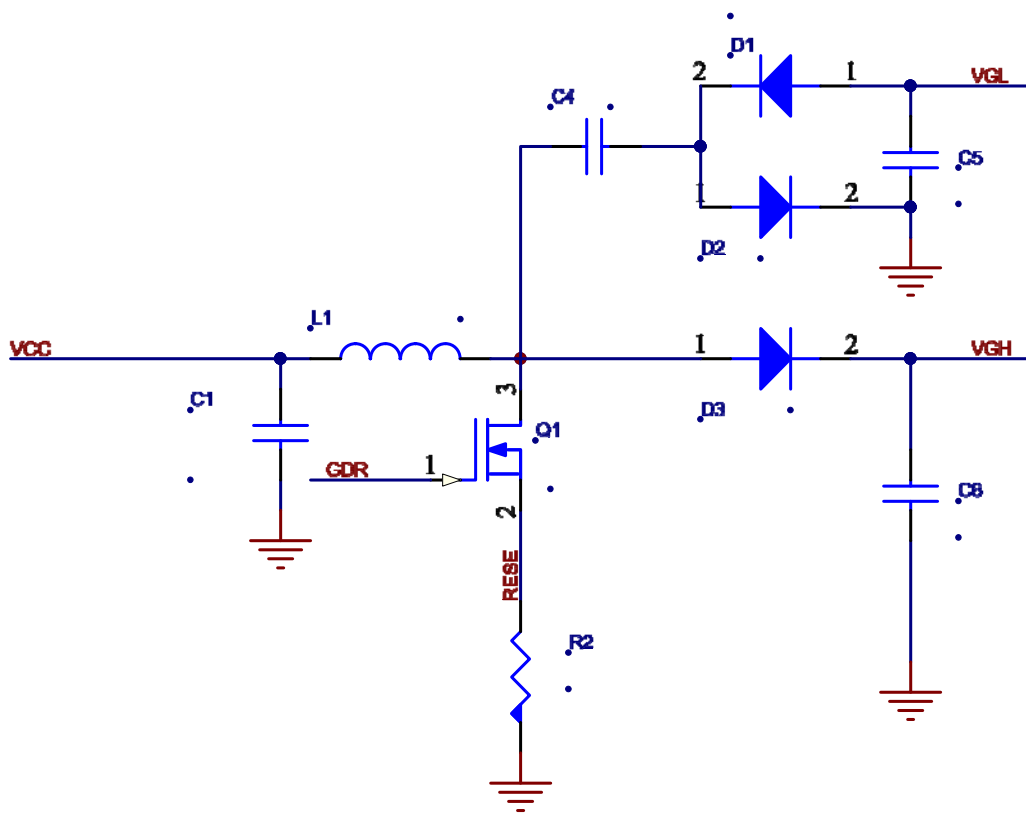


Figure. 10-2

Part Name	Value /requirement/Reference Part
C1—C3	1uF/0603;X5R/X7R;Voltage Rating: 25V
C4	4.7uF/0603;X5R/X7R;Voltage Rating: 25V
C5-C10	1uF/0603;X5R/X7R;Voltage Rating: 25V
D1—D3	MBR0530 1) Reverse DC voltage $\geq 30V$ 2) Forward current $\geq 500mA$ 3)Forward voltage $\leq 430mV$
R2	0.47 Ω /0603: 1% variation
Q1	NMOS:Si1308EDL 1) Drain-Source breakdown voltage $\geq 30V$ 2) V_{gs} (th) =0.9 (Typ) , 1.3V (Max) 3) $R_{ds\ on} \leq 2.1 \Omega$ @ $V_{gs}=2.5V$
L1	10uH/Taiyo Yuden NR4018T100M DCR<0.5 ohm, Isat $\geq 1.2A$ @ 25° C
CON24Pin	0.5mm ZIF Socket 24Pins,0.5mm pitch



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11. ABSOLUTE MAXIMUM RATING

Table 12-1: Maximum Ratings

Symbol	Parameter	Rating	Unit	Humidity	Unit	Note
V _{CI}	Logic supply voltage	-0.5 to +6.0	V	-	-	
T _{OPR}	Operation temperature range	0 to 50	°C	35 to70	%	
T _{ttg}	Transportation temperature range	-25 to 60	°C	-	-	Note11-2
T _{stg}	Storage condition	0 to 40	°C	35 to70	%	Maximum storage time: 5 years

Note 11-1:Maximum ratings are those values beyond which damages to the device may occur.

Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

Note11-2: T_{ttg} is the transportation condition, the transport time is within 10 days for -25°C~0°C or 50°C~60°C.

12.DC CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.3V, T_{OPR}=25°C.

Table 12-1: DC Characteristics

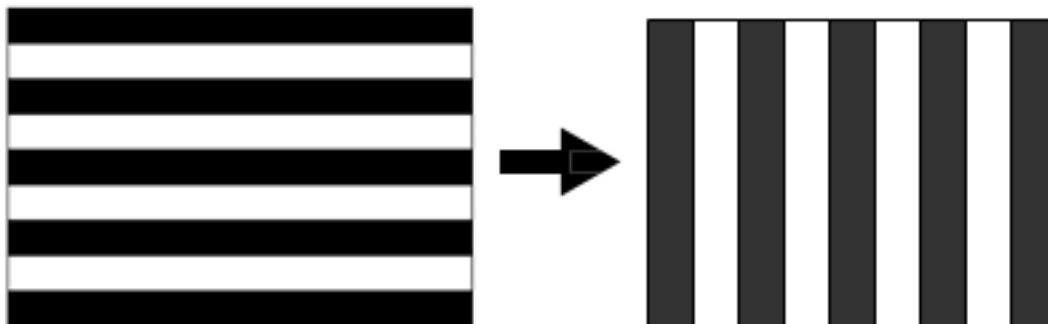
Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
VDD	VDD operation voltage		VDD	2.5	3.3	3.6	V
VIH	High level input voltage		SDA, SCL, CS#, D/C#, RES#, BS1	0.7VDDIO		VDDIO	V
VIL	Low level input voltage			0		0.3VDDIO	V
VOH	High level output voltage	IOH = 400uA	BUSY	VDDIO-0.4			V
VOL	Low level output voltage	IOL = -400uA		0		0.4	V
Iupdate	Module operating current			-	5	-	mA
Isleep	Deep sleep mode	VCI=3.3V		-	-	3	uA

The Typical power consumption is measured using associated 25°C waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 12-1)

- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by XingTai.
- Vcom value will be OTP before in factory or present on the label sticker.

Note 12-1

The Typical power consumption





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13. AC Characteristics

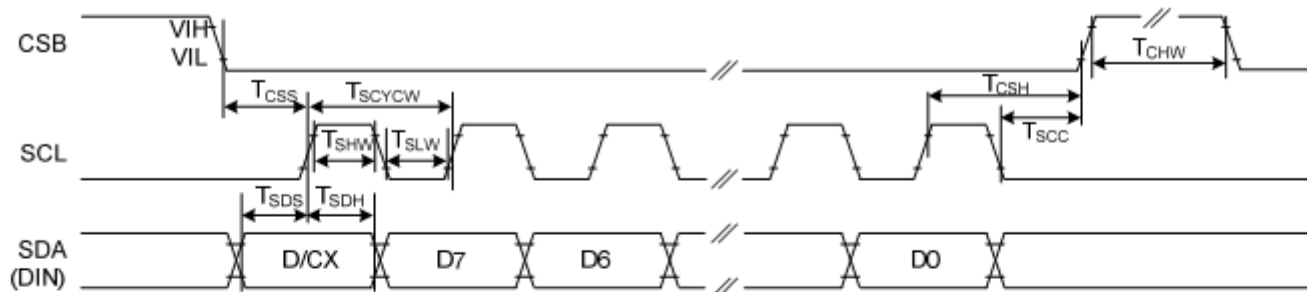


Figure: 3-wire Serial Interface Characteristics (Write mode)

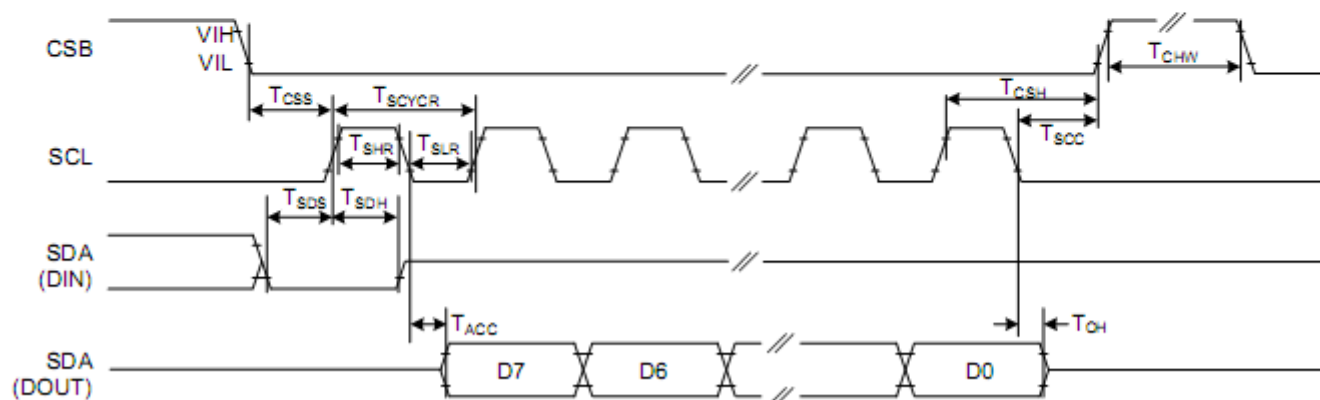


Figure: 3-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL "H" pulse width (Write)	35			ns
T_{SLW}		SCL "L" pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	350			ns
T_{SHR}		SCL "H" pulse width (Read)	175			ns
T_{SLR}		SCL "L" pulse width (Read)	175			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			350	ns
T_{OH}		Output disable time	15			ns



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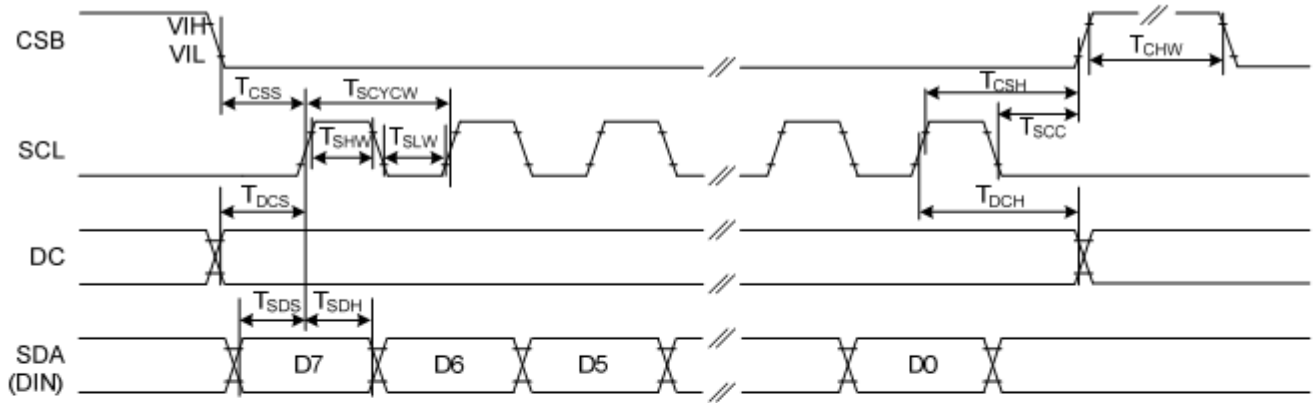


Figure: 4-wire Serial Interface Characteristics (Write mode)

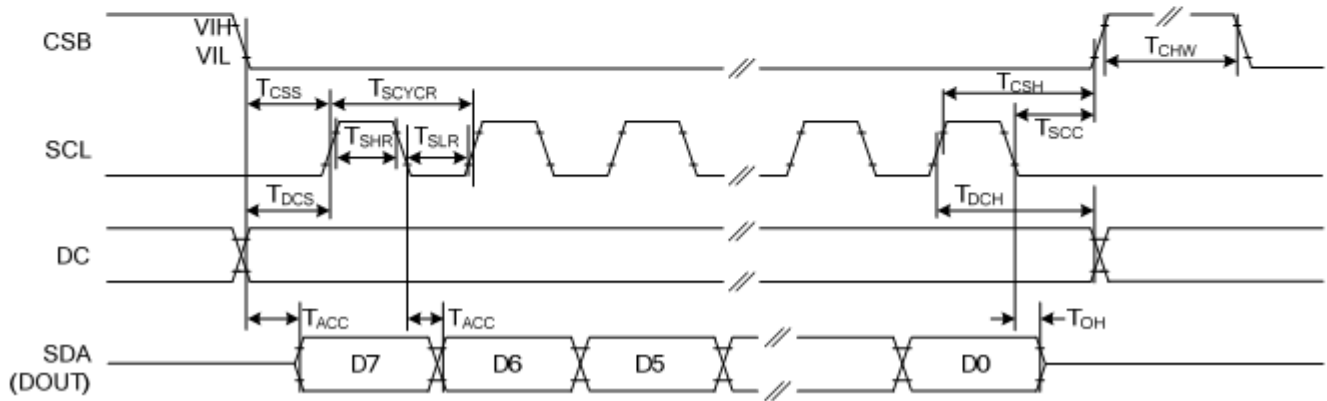


Figure: 4-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
$T_{SCYC W}$	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL "H" pulse width (Write)	35			ns
T_{SLW}		SCL "L" pulse width (Write)	35			ns
$T_{SCYC R}$		Serial clock cycle (Read)	350			ns
T_{SHR}		SCL "H" pulse width (Read)	175			ns
T_{SLR}		SCL "L" pulse width (Read)	175			ns
T_{DCS}	DC	DC setup time	30			ns
T_{DCH}		DC hold time	30			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			350	ns
T_{OH}		Output disable time	15			ns



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14. Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25°C	-	50	mAs	-
Deep sleep mode	-	25°C	-	3	uA	-

MAS=update average current ×update time

15.Optical characteristics

15.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25±3°C, VCI=3.3V

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 17-1
Gn	2 Grey level	-	-	-	-	L*	-
CR	Contrast Ratio	-	-	10	-	-	-
Panel	Image Update	Storage and transportation	-	Update the white screen	-	-	-
	Update Time	Operation	-	Suggest Updated once a day	-	-	-

WS : White state, KS : Black state,

Note 15-1 : Luminance meter : i - One Pro Spectrophotometer

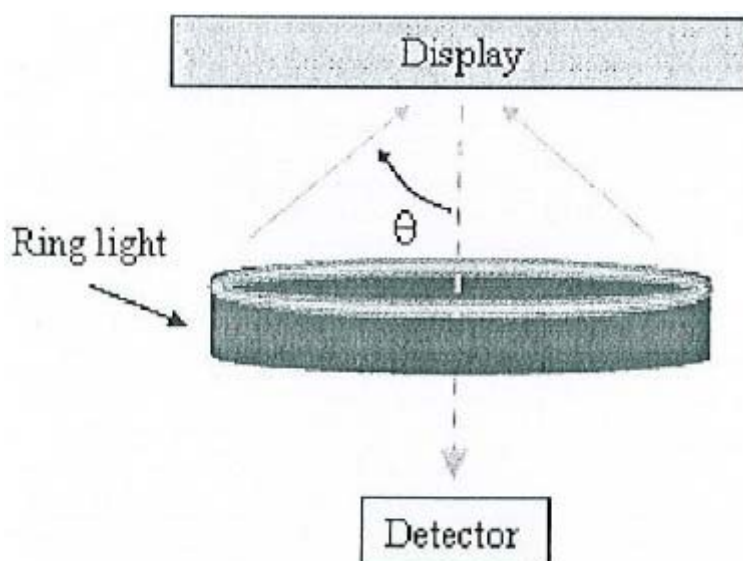
15.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd)():

R1: white reflectance

Rd: dark reflectance

$$CR = R1/Rd$$





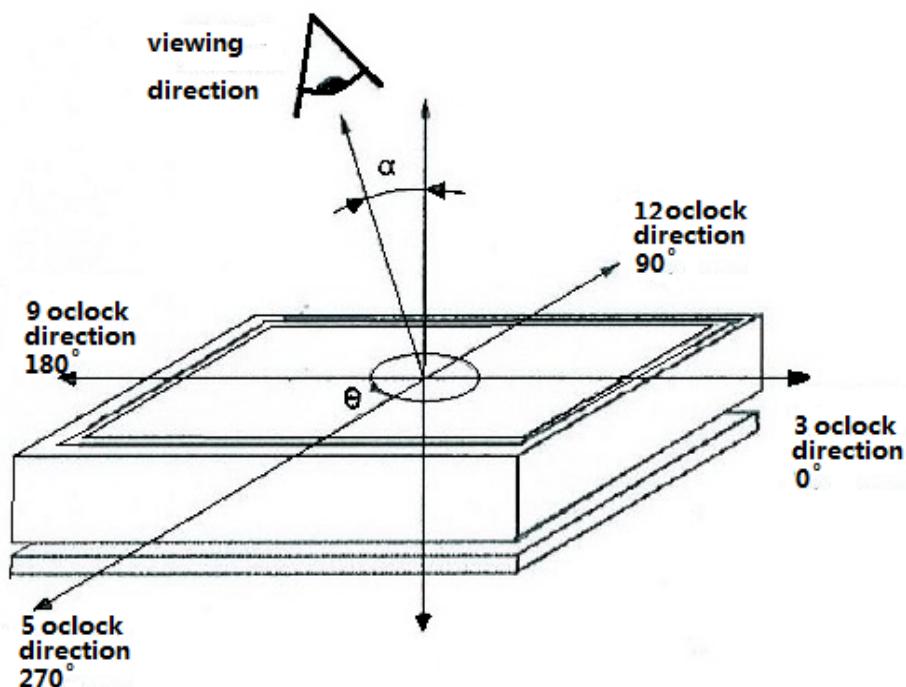
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15.3 Reflection Ratio

The reflection ratio is expressed as:

$$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$$

L_{center} is the luminance measured at center in a white area ($R=G=B=1$). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.





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16. HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display module should be kept flat or fixed to a rigid, curved support with limited bending along the long axis. It should not be used for continual flexing and bending. Handle with care. Should the display break do not touch any material that leaks out. In case of contact with the leaked material then wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.
Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions
(1) It's recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It's recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	The data sheet contains final product specifications.



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Limiting values			
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.			
Application information			
Where application information is given, it is advisory and dose not form part of the specification.			

Product Environmental certification
ROHS
REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.



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17. Reliability test

17.1 Reliability test item

	TEST	CONDITION	REMARK
1	High-Temperature Operation	T=40℃, RH=35%RH, For 240Hr	
2	Low-Temperature Operation	T = 0℃ for 240 hrs	
3	High-Temperature Storage	T=60℃ RH=35%RH For 240Hr	Test in white pattern
4	Low-Temperature Storage	T = -25℃ for 240 hrs	Test in white pattern
5	High Temperature, High-Humidity Operation	T=40℃, RH=90%RH, For 168Hr	
6	High Temperature, High-Humidity Storage	T=60℃, RH=80%RH, For 240Hr	Test in white pattern
7	Temperature Cycle	-25℃(30min)~70℃(30min), 100 Cycle	Test in white pattern
8	Package Vibration	1.04G, Frequency : 20~200Hz Direction : X,Y,Z Duration: 30 minutes in each direction	Full packed for shipment
9	Package Drop Impact	Drop from height of 100 cm on Concrete surface Drop sequence: 1 corner, 3 edges, 6 face One drop for each.	Full packed for shipment
10	UV exposure Resistance	765 W/m ² for 168hrs, 40℃	
11	Electrostatic discharge	Machine model: +/-250V, 0Ω, 200pF	No operation

Actual EMC level to be measured on customer application.

Note1: Stay white pattern for storage and non-operation test.

Note2: Operation is black/white pattern, hold time is 150S.

Note3: The function, appearance, opticals should meet the requirements of the test before and after the test.

Note4: Keep testing after 2 hours placing at 20℃-25℃.

17.2 Product warranty

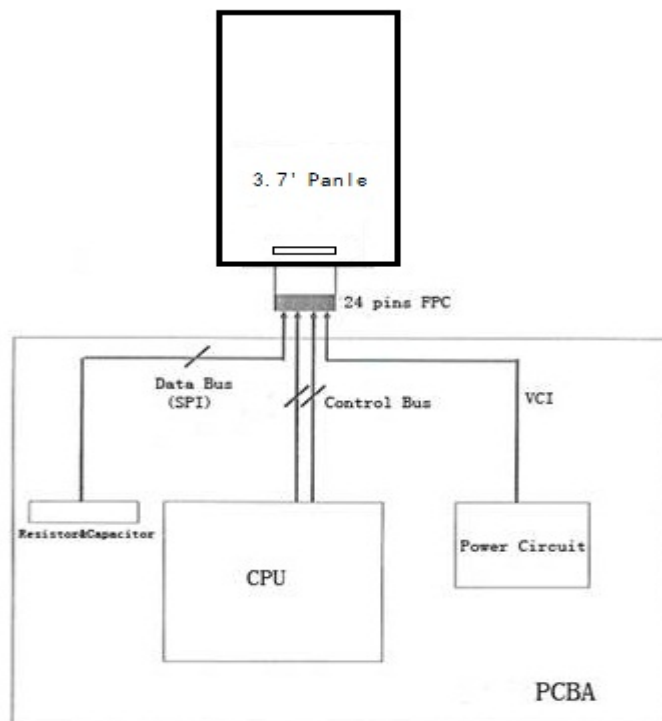
Warranty conditions have to be negotiated between Xingtai and individual customers.

Xingtai provides 12+1(one month delivery time) months warranty for all products which are purchased from Xingtai.

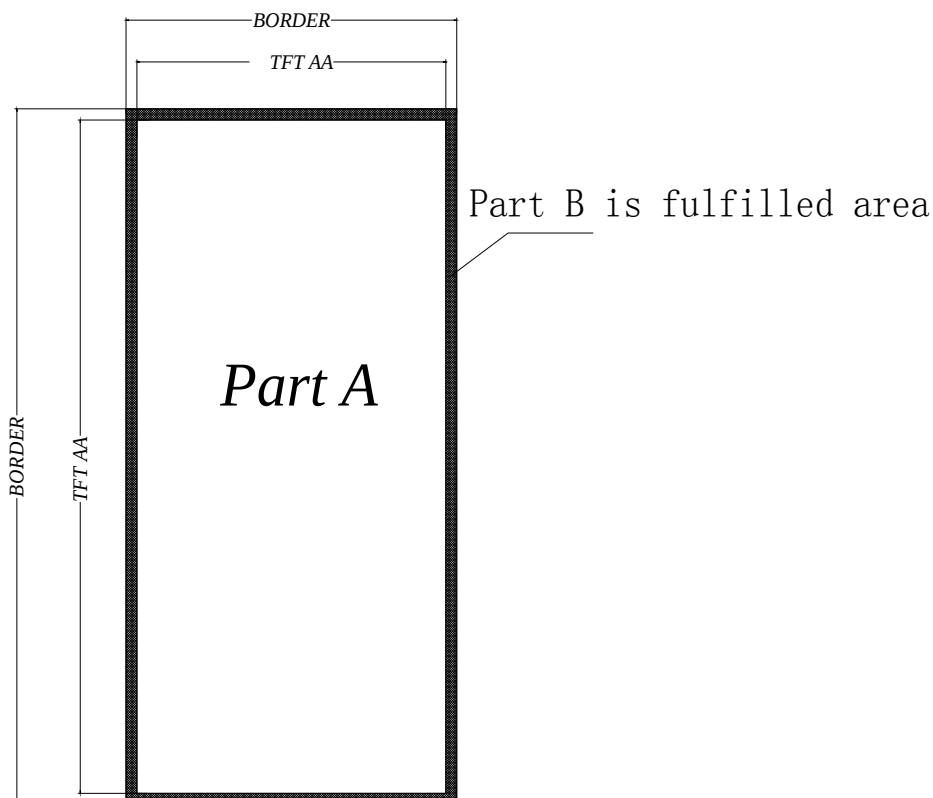


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18. Block Diagram



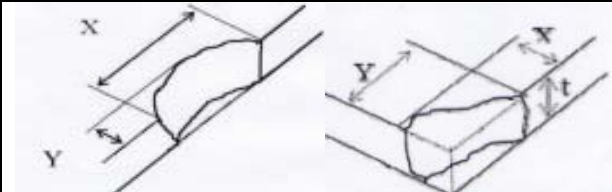
19. PartA/PartB specification





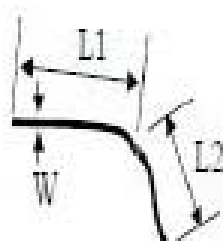
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20. Point and line standard

Shipment Inspection Standard						
Equipment: Electrical test fixture, Point gauge						
Outline dimension	53(H) × 92.99(V) × 0.9(D)	Unit: mm	Part-A	Active area	Part-B	Border area
Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	19℃～25℃	55%±5%RH	800～1300Lux	300 mm	35Sec	
Defet type	Inspection method	Standard		Part-A		Part-B
Spot	Electric Display	D≤0.25 mm		Ignore		Ignore
		0.25 mm<D≤0.4 mm		N≤4		Ignore
		D>0.4 mm		Not Allow		Ignore
Display unwork	Electric Display	Not Allow		Not Allow		Ignore
Display error	Electric Display	Not Allow		Not Allow		Ignore
Scratch or line defect(include dirt)	Visual/Film card	L≤2 mm, W≤0.2 mm		Ignore		Ignore
		2.0mm<L≤5.0mm, 0.2<W≤0.3mm,		N≤2		Ignore
		L>5 mm, W>0.3 mm		Not Allow		Ignore
PS Bubble	Visual/Film card	D≤0.2mm		Ignore		Ignore
		0.2mm≤D≤0.35mm & N≤4		N≤4		Ignore
		D>0.35 mm		Not Allow		Ignore
Side Fragment	Visual/Film card	X≤6mm, Y≤0.4mm, Do not affect the electrode circuit (Edge chipping)				
		X≤1mm, Y≤1mm, Do not affect the electrode circuit((Corner chipping)				
		Ignore				
						
Remark	1. Appearance defect should not cause electrical defects;					
	2. Appearance defects should not cause dimensional accuracy problems					
	L=long W=wide D=point size N=Defects NO					

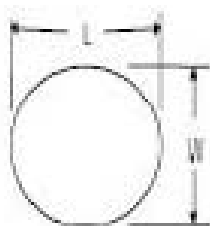


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$L = L1 + L2$

Line Defect



$D = (L + W) / 2$

Spot Defect

L=long W=wide D=point size



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21. Barcode

21.1 label appearance



ABBBBBBBCC
DDDEEEFGGG

21.2 QR scanned information (Total 28 code number+ 2 blank spaces)

A BBBBBBBB CC □ DDD EEE F GGG □ H III JJ KK
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪

- ① A——The factory code
- ② BBBBBBBB——Module name of EPD
- ③ CC——Production line
- ④ DDD——Date of production
- ⑤ EEE——Production lot
- ⑥ F——Separator
- ⑦ GGG——FPL Lot
- ⑧ H——Normal Lot
- ⑨ III——TFT、PS、EC.
- ⑩ JJ——IC
- ⑪ KK——Serial NO.



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22. Packing

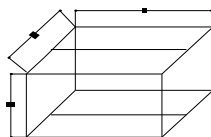
Packing Spec

Sheet No:

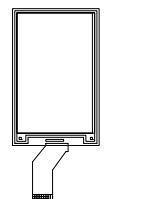
	Part No	HINK-E037A04	DATE	2019. 11. 29	VER	A0	Page	2-1
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一, Package Type: Box

Box No	HINK-E037A03-ZX-A0
Box size	515*322*170
Containment	144 PCS



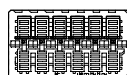
PRODUCT DRAWING



二, Inside package type: Plastic

Tray unit: mm

Plastic Tray	465*280*15	13 pcs
Anti-static foil bags	700*530*0.1	1 pcs
EPE (inside)	408.17*114.75*2	12 pcs
EPE (Up-Down)	485*145*10	2 pcs
EPE (Left-Right)	285*480*10	2 pcs
EPE (Front-back)	310*145*10	2 pcs
Chip board	500*306*5	2 pcs
Quantity/tray	12 pcs	
Tray number/sheet	12+1 Sheets	
Box	1	



Empty tray

Anti-static EPE

Step 1:

Material: Tray, EPE
Put the product in to the tray and keep the display side up. Then put anti-static EPE in to each holes.

Step 2,

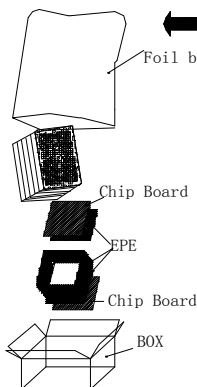
1), Must keep the angle 180 degree placed between the neighboring Plastic trays.
2), There are 12 layers product, total 4*12=48 pcs.
3), An empty Plastic tray intersects put on the top of the plastic trays.

Step 5,

1), Seal the box with adhesive tapes.
2), Paste the lable onto the exterior box, and the lable can't cover the safety, transfer and RoSH sign.

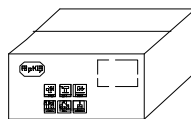
Step 3,

1), In each case, put 2 bags of desiccant, then seal the trays with adhesive tapes.
2), Put the trays into foil bags.
3), heat seal the foil bags.



Step 4,

1), First put a chip board on the bottom of the box, then placed the down EPE, the left-right and front-back EPE.
2), Placed the sealed products into the box.
3), The last placed the up EPE on the top of the trays, and place a chip board on it.



Design	C. X. Y	Approve	X. B	Confirm	H. Z. P
Date	2019. 11. 29	Date	2019. 11. 29	Date	2019. 11. 29