



File Name	Specification For 28.0" EPD	Module Number	T280A03
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Specification for 28.0"EPD

Model NO.: T280A03

Product VER: A0

Customer Approval

Customer	
Approval By	
Date Of Approval	

It will be agreed by the receiver, if not sign back the Specification within 15days.

Prepared By	Checked By	Approval By
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Version	Content	Date	Producer
A0	New release	2025/7/21	Leslie



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1. General Description

T280A03 is a reflective electrophoretic E Ink® Spectra 6 technology display module based on active matrix TFT substrate. It has 28" active area with 3840*1080 pixels and 32 : 9 aspect ratios. The display is capable to display images at Black/White/Red/Yellow/Blue/Green depending on the display controller and the associated waveform file it used.

2. Features

- 3840*1080 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Display Black/White/Red/Yellow/Blue/Green colors
- High contrast electrophoretic imaging film
- Pure reflective mode
- Bi-stable image
- Portrait mode
- Operation temperature range: 0°C~50°C

3. General Specifications

Parameter	Specifications	Unit	Remark
Screen Size	28	Inch	32:9
Display Resolution	3840(H) x 1080(V)	Pixel	Dpi:143ppi
Active Area	683.52(H)x 192.24(V)	mm	
Pixel Pitch	0.178*0.178	mm	
Pixel Configuration	Square		
Outline Dimension	698.6H)x209.3(V)x0.82(D)	mm	Without masking film
Weight	TBD	g	



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5. Input / Output Interface

5-1) Connector type

Item	Pin numbers	Pitch (mm)	Connector	Note
CN1	51	0.5	P-TWO 187059-51221-1	LVDS Type
CN2	51	0.5	P-TWO 187059-51221-1	LVDS Type

5-2) Pin Assignment

Connector CN1

Pin #	Signal	I/O	Description	Remark
1	VCOM	P	Common Voltage.	
2	VCOM	P	Common Voltage.	
3	VCOM	P	Common Voltage.	
4	NC	-	NO Connection	
5	VCOM	P	Common Voltage.	
6	VCOM	P	Common Voltage.	
7	NC	-	NO Connection	
8	BORDER	P	Border connection	
9	NC	-	NO Connection	
10	VGH	P	Positive power supply gate driver.	
11	VGH	P	Positive power supply gate driver.	
12	NC	-	NO Connection	
13	VP3	P	Positive power supply source driver.	
14	VP3	P	Positive power supply source driver.	
15	VP3	P	Positive power supply source driver.	
16	NC	-	NO Connection	
17	VP2	P	Positive power supply source driver.	
18	VP2	P	Positive power supply source driver.	
19	VP2	P	Positive power supply source driver.	
20	NC	-	NO Connection	
21	VP1	P	Positive power supply source driver.	
22	VP1	P	Positive power supply source driver.	
23	VP1	P	Positive power supply source driver.	



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24	NC	-	NO Connection		
25	VDD	P	Logic power.		
26	VDD	P	Logic power.		
27	NC	-	NO Connection		
28	VSS	P	Ground		
29	VSS	P	Ground		
30	NC	-	NO Connection		
31	VN1	P	Negative power supply source driver.		
32	VN1	P	Negative power supply source driver.		
33	VN1	P	Negative power supply source driver.		
34	NC	-	NO Connection		
35	VN2	P	Negative power supply source driver.		
36	VN2	P	Negative power supply source driver.		
37	VN2	P	Negative power supply source driver.		
38	NC	-	NO Connection		
39	VN3	P	Negative power supply source driver.		
40	VN3	P	Negative power supply source driver.		
41	VN3	P	Negative power supply source driver.		
42	NC	-	NO Connection		
43	VGL	P	Negative power supply gate driver.		
44	VGL	P	Negative power supply gate driver.		
45	NC	-	NO Connection		
46	NC	-	NO Connection		
47	NC	-	NO Connection		
48	NC	-	NO Connection		
49	STBYB	I	mini-LVDS enable.		
50	XON	I	XON signal gate driver		
51	MODE	I	Output enable gate driver		

Connector CN2

Pin #	Signal	I/O	Description	Remark
1	DSEL	I	Data Input select	
2	LEH	I	Latch enable source driver	
3	OEH	I	Outputs enabled when OE is logic "H", Outputs forced to GND when OE is logic "L".	



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4	UD	I	Shift direction control pin gate driver UD = H: Data shift direction from G1 to G800. UD = L: Data shift direction from G800 to G1.	
5	SHR	I	Shift direction control pin source driver SHR =H: Data inputs read sequentially from S800 to S1. SHR =L: Data inputs read sequentially from S1 to S800.	
6	SPV2	I/O	Start pulse gate driver	
			UD	Start pulse input Start pulse output
			H	SPV1 SPV2
			L	SPV2 SPV1
7	SPV1	I/O	Start pulse gate driver	
			UD	Start pulse input Start pulse output
			H	SPV1 SPV2
			L	SPV2 SPV1
8	SPH2	I/O	Start pulse source driver	
			SHR	Start pulse input Start pulse output
			H	SPH2 SPH1
			L	SPH1 SPH2
9	SPH1	I/O	Start pulse source driver	
			SHR	Start pulse input Start pulse output
			H	SPH2 SPH1
			L	SPH1 SPH2
10	VSS	P	Ground	
11	CKV	I	Clock gate driver	
12	VSS	P	Ground	
13	LV11N	I	Data signal source driver	
14	LV11P	I	Data signal source driver	
15	VSS	P	Ground	
16	LV10N	I	Data signal source driver	
17	LV10P	I	Data signal source driver	
18	VSS	P	Ground	
19	LV9N	I	Data signal source driver	
20	LV9P	I	Data signal source driver	
21	VSS	P	Ground	
22	LV8N	I	Data signal source driver	

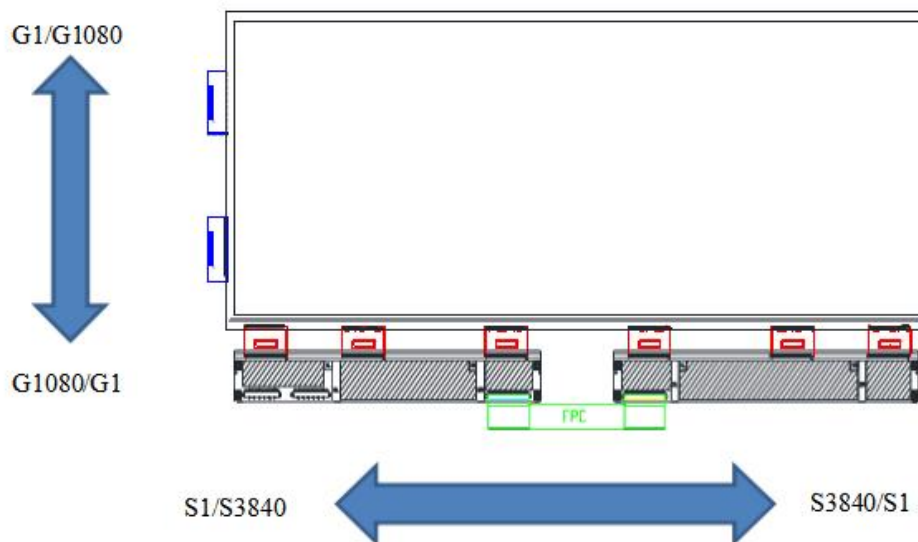


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23	LV8P	I	Data signal source driver		
24	VSS	P	Ground		
25	LV7N_D15	I	Data signal source driver		
26	LV7P_D14	I	Data signal source driver		
27	VSS	P	Ground		
28	LV6N_D13	I	Data signal source driver		
29	LV6P_D12	I	Data signal source driver		
30	VSS	P	Ground		
31	CLKN_GLOSTL	I	Data signal source driver		
32	CLKP_CKH	I	Data signal source driver		
33	VSS	P	Ground		
34	LV5N_D11	I	Data signal source driver		
35	LV5P_D10	I	Data signal source driver		
36	VSS	P	Ground		
37	LV4N_D9	I	Data signal source driver		
38	LV4P_D8	I	Data signal source driver		
39	VSS	P	Ground		
40	LV3N_D7	I	Data signal source driver		
41	LV3P_D6	I	Data signal source driver		
42	VSS	P	Ground		
43	LV2N_D5	I	Data signal source driver		
44	LV2P_D4	I	Data signal source driver		
45	VSS	P	Ground		
46	LV1N_D3	I	Data signal source driver		
47	LV1P_D2	I	Data signal source driver		
48	VSS	P	Ground		
49	LV0N_D1	I	Data signal source driver		
50	LV0P_D0	I	Data signal source driver		
51	VSS	P	Ground		



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5-3) Panel Scan Directions



6. Electrical Characteristics

6-1 Absolute Maximum Ratings:

Parameter	Symbol	Rating	Unit	Remark
Logic Supply Voltage	VDD	-0.3 to +5.0	V	
Source Positive Supply Voltage	VP3	-0.3 to VN3+50	V	
Source Positive Supply Voltage	VP2	-0.3 to VP3	V	
Source Positive Supply Voltage	VP1	-0.3 to VP3	V	
Source Negative Supply Voltage	VN1	VN3 to + 0.3	V	
Source Negative Supply Voltage	VN2	VN3 to + 0.3	V	
Source Negative Supply Voltage	VN3	-25 to + 0.3	V	
Gate Positive Supply Voltage	VGH	-0.3 to +55	V	
Gate Negative Supply Voltage	VGL	-32 to +0.3	V	
Supply Range	VGH-VGL	-0.3 to +55	V	
Operating Temp. Range	TOTR	-15 to +65	°C	
Storage Temperature	TSTG	-25 to +70	°C	



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6-2 Panel DC characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal Ground	VSS			0		V
Logic voltage Supply	VDD		2.7	3.3	3.6	V
	IDD	VDD = 3.3V		45.60	67.82	mA
Gate Negative Supply	VGL		-21	-20	-19	V
	IGL	VGL = -20V		7.93	18.61	mA
Gate Positive Supply	VGH		26	27	28	V
	IGH	VGH = 27V		6.00	7.47	mA
Source Negative Supply	VN1		-16	-15	-14	V
	IN1	VN1 = -15V		13.84	682.28	mA
Source Negative Supply	VN2 *(Note 9)		-13	-12	-11	V
	IN2	VN2 = -12V		1.89	2.80	mA
Source Negative Supply	VN3		-21	-20	-19	V
	IN3	VN3 = -20V		13.15	84.20	mA
Source Positive Supply	VP1		14	15	16	V
	IP1	VP1 = 15V		9.80	646.85	mA
Source Positive Supply	VP2 *(Note 9)		11	12	13	V
	IP2	VP2 = 12V		2.31	13.17	mA
Source Positive Supply	VP3		19	20	21	V
	IP3	VP3 = 20V		1.31	31.37	mA
Border Supply	-		-	-	-	V

Asymmetry Source	Vasm	VP1+VN1	-800		800	mV
Common Voltage	VCOM		-3.5	Adjusted	-0.3	V
	ICOM			16.02	18.70	mA
Maximum Power panel	Pmax				23237	mW
Typical power panel	Ptyp			1165		mW
Standby power panel	Pstby				60.2	mW



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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum Currents (*Note 5)	IP1	VP1 = 15V	-		1500	mA
	IN1	VN1 = -15V	-		1540	mA
	IGH	VGH = 27V	-		416	mA
	IGL	VGL = -20V	-		1220	mA
	ICOM		-		4000	mA

Note:

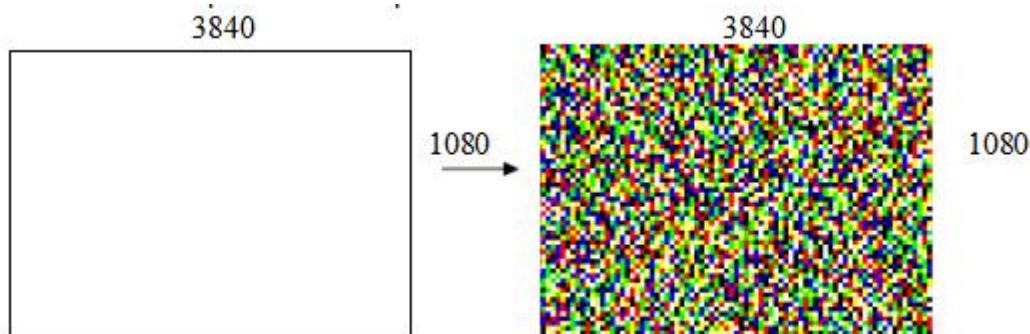
- The maximum power consumption is measured using 75Hz waveform with following pattern transition: from pattern of repeated 1 consecutive black scan lines followed by 1 consecutive white scan line to that of repeated 1 consecutive white scan lines followed by 1 consecutive black scan lines. (Note A-1)
- The Typical average current for power consumption is measured using 75 Hz waveform with following pattern transition: from horizontal 4 gray scale pattern to vertical 4 gray scale pattern. (Note A-2)
- The standby power is the consumed power when the panel controller is in standby mode.
- The maximum power consumption is measured using 75Hz waveform with following pattern transition: from pattern of repeated 1 consecutive black scan lines followed by 1 consecutive white scan line to that of repeated 1 consecutive white scan lines followed by 1 consecutive black scan lines.
 - It is performed with decoupling capacitors on each power rail as below table (Note A-3).
 - The minimum value in table of Maximum current is produced by charging mechanism between decoupling capacitors.
- The listed electrical/optical characteristics are only guaranteed under the controller and waveform provided by E Ink.
- Vcom is recommended to be set in the range of assigned value ± 0.1 V
- Use of measuring instruments: Oscilloscope (Model: Tektronix MDO3024)
- The maximum current is for reference only.
- VP2/VN2 of source supply are only for source driver IC requirement, the value will be different base on power design circuit in hardware, the value range can refer to 6-1) Absolute maximum rating.



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Note 6-1

The typical power consumption



Note 6-2

The high loading power consumption



Note 6-3

The decoupling capacitors on each power rail for Max. Currents

Power rail	Capacitors suggested (uF / Tolerance)
IDD	2.2uF x 14pcs / ±10%
IP1	2.2uF x 12pcs / ±10%
IP2	2.2uF x 12pcs / ±10%
IP3	2.2uF x 12pcs / ±10%
IN1	2.2uF x 12pcs / ±10%
IN2	2.2uF x 12pcs / ±10%
IN3	2.2uF x 12pcs / ±10%
IGH	2.2uF x 2pcs / ±10%
IGL	2.2uF x 3pcs / ±10%
ICOM	No Capacitor



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6-4) Refresh Rate

The module ED280TT1 is applied at a maximum screen refresh rate of 75Hz.

	Min	Max
Refresh Rate	-	75 Hz

6-5 Panel AC Characteristics

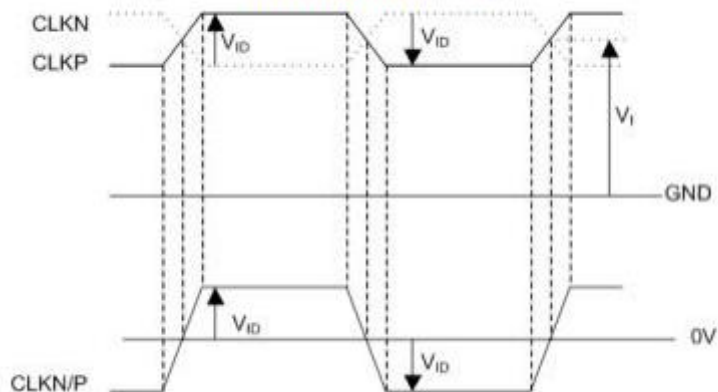
VDD=2.7V to 3.6V, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit
mini-LVDS differential voltage	V_{ID}	300	-	-	mV
mini-LVDS common mode input voltage range	V_I	0.4	1.0	VDD-1.4	V
Source Clock frequency	F_{CLK}	-	-	150	MHz
Source Clock setup time	t_{SETUP1}	1.1	-	-	ns
Source Clock hold time	t_{HOLD1}	1.1	-	-	ns
Rise time	t_{RISE}	-	-	0.15	Unit interval
Fall time	t_{FALL}	-	-	0.15	Unit interval
LE rising to reset input time	$t_{LE-RESET_HIGH}$	200	-	-	ns
LE falling to reset input time	$t_{LE-RESET_LOW}$	200	-	-	ns
Reset high period	t_{RESETH}	3	-	-	CLK
Receiver off to LE timing	$t_{REC-OFF}$	40	-	-	CLK
LE width	t_{LE}	300	-	-	ns
Gate clock pulse high period	t_{CLKH}	500	-	-	ns
Gate clock pulse low period	t_{CLKL}	500	-	-	ns
Gate clock rise time	t_{IR_CLK}	-	-	100	ns
Gate clock fall time	t_{IF_CLK}	-	-	100	ns
Gate Start pulse setup time	t_{SU}	100	-	$t_{CLKH}-100$	ns
Gate Start pulse hold time	t_{HD}	100	-	$t_{CLKL}-100$	ns
Gate Start pulse rise time	t_{IR_STV}	-	-	100	ns
Gate Start pulse fall time	t_{IF_STV}	-	-	100	ns

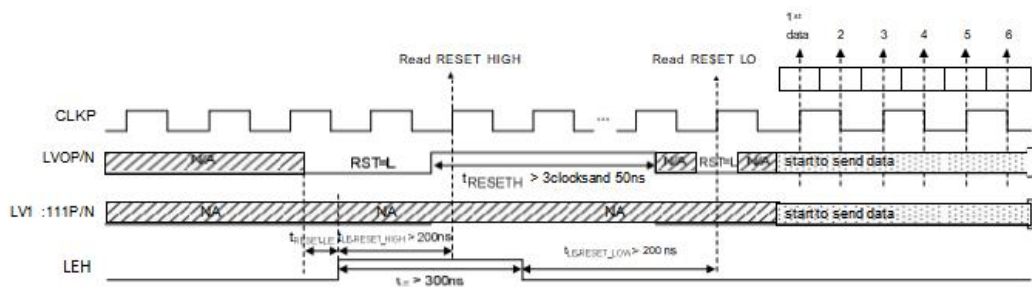
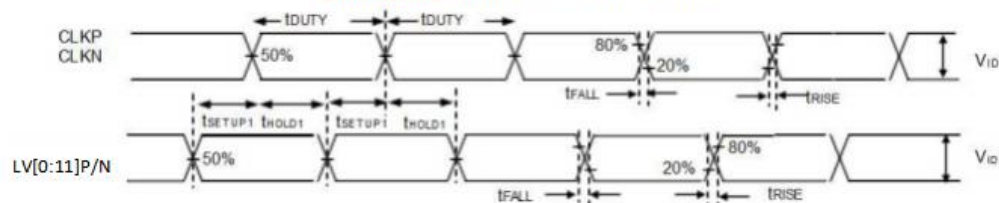


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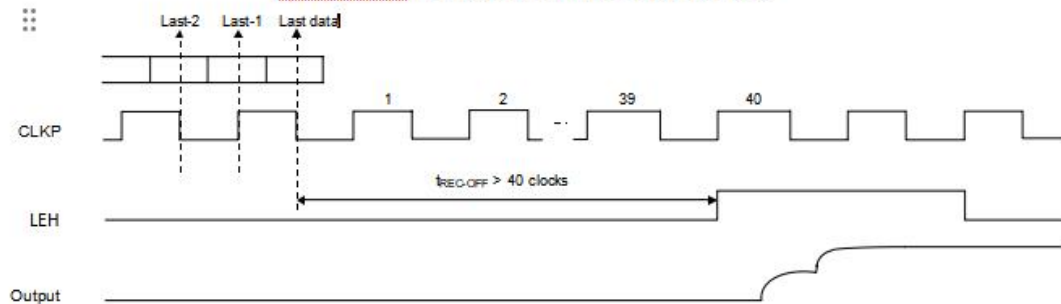
Mini-LVDS clock

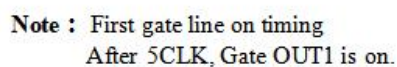


Mini-LVDS timing for receiving data



Mini-LVDS last data sampling to LE timing





The timing mode is depicted on Figure 6.1 and it refers to timing of Source Driver Output Enable (SDOE) and Gate Driver Clock (GDCK). Note, the controller timing in the mode LGON follows GDCK timing.

The diagram illustrates the timing of various signals for the first frame (Frame 1-N). The signals shown are:

- Vsync**: Vertical sync signal.
- SPV**: Signal processing vertical clock, showing fields FSL, FBL, FDL, ..., FEL.
- Hsync (CKV)**: Horizontal sync signal (CKV), showing lines Line1, Line2, ..., Line180.
- OEH**: Output enable high signal.
- MODE**: Mode signal.
- Hsync (CKV)**: Horizontal sync signal (CKV), showing GATE_OFF, GATE_ON = LGONL, and GATE_OFF.
- CLKP**: Clock signal.
- LEH**: Load enable high signal.
- LVDP/N**: Load vertical data port signal, showing a period of 3 CLKP and 50ns.
- LV[1:1]P/N**: Load vertical data port signal, showing a period of 3 CLKP and 50ns.
- LSL**: Load start line.
- LBL**: Load blanking line.
- LDL**: Load data line.
- LEL**: Load end line.
- GDCK_STA**: Gate clock start signal.

A red arrow points to the 'Scan Line' between Line1 and Line2.

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Mode	3	Resolution 3840 x 1080				
SDCK [MHz]	48					
Pixels Per SDCK	8					
Line Parameters [SDCK]	LSL	LBL	LDL	LEL	GDCK_STA	LGONL
	15	15	480	79	1	466
Line Parameters [us]	0.31	0.31	10	1.65	0.02	9.71
Frame Parameters [lines]	FSL	FBL	FDL	FEL	-	FR [Hz]
	1	4	1080	1	-	75
Frame Parameters [us]	12.27	47.92	23090.4	11.38	-	-
					-	-



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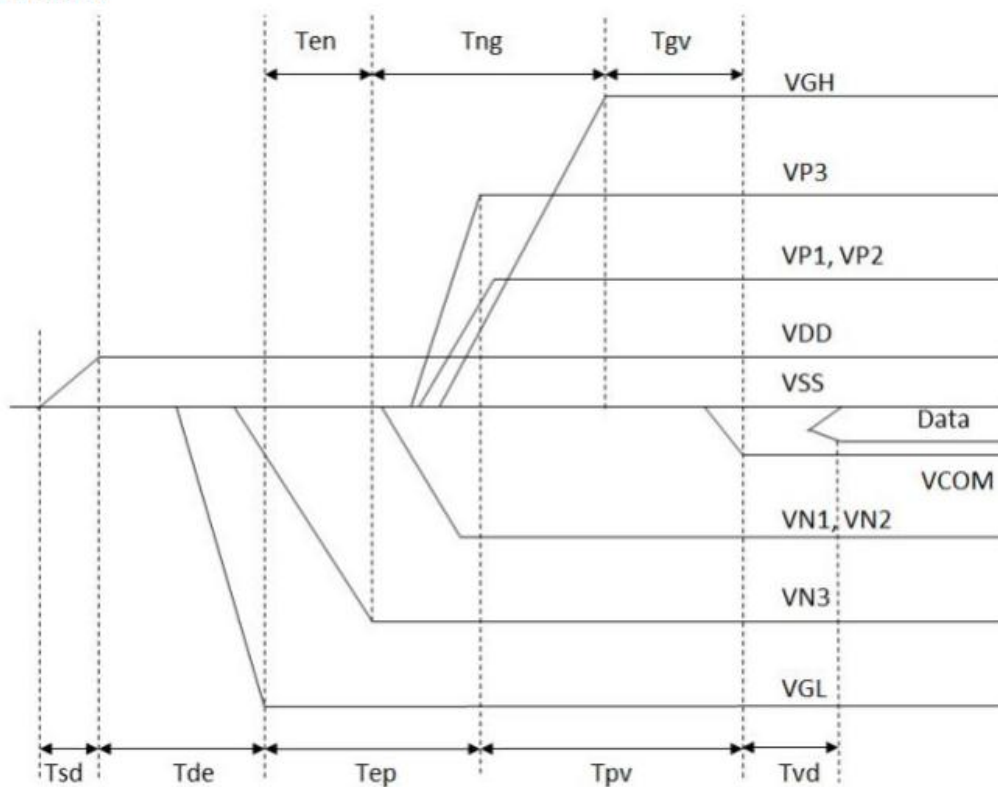
7. Power Sequence

Power Rails must be sequenced in the following order :

1. VSS → VDD → VN3 → VN1(VN2) → VP1(VP2) → VP3 → VCOM

2. VSS → VDD → VGL → VGH (Gate driver)

POWER ON

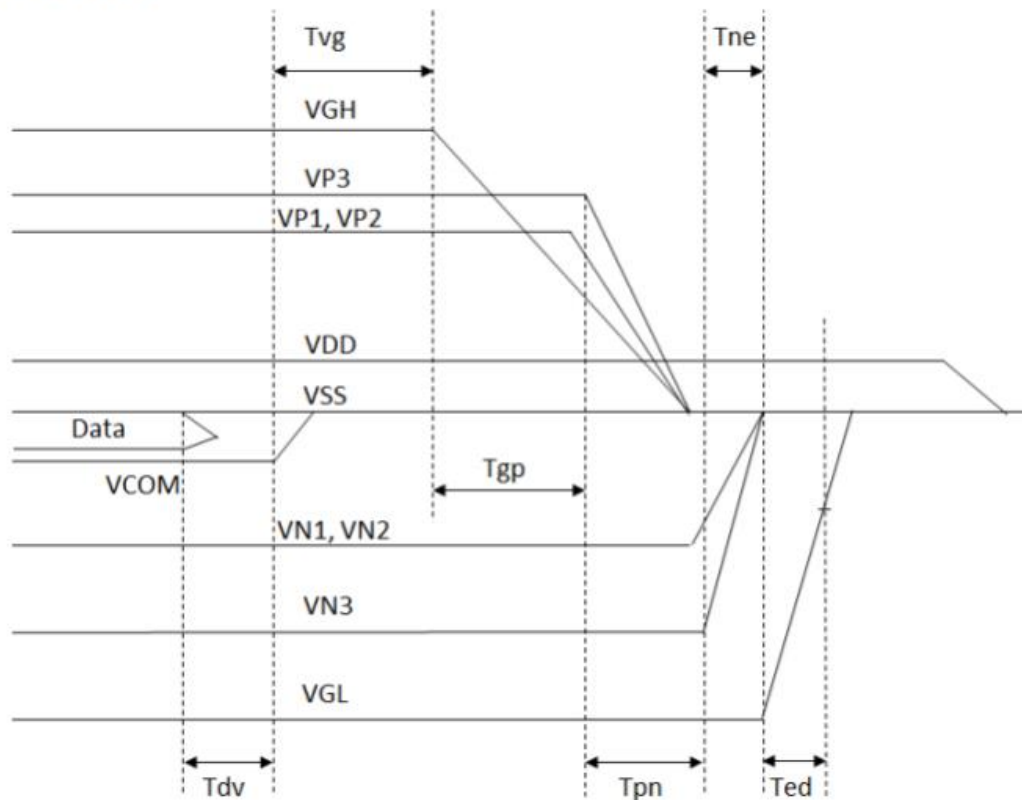


	Min	Max	Remark
Tsd	30us	-	
Tde	100us	-	
Tep	1000us	-	
Tpv	100us	-	
Tvd	100us	-	
Ten	0us	-	
Tng	1000us	-	
Tgv	100us	-	



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POWER OFF



	Min	Max	Remark
Tdv	100μs	-	-
Tvg	0μs	-	-
Tgp	0μs	-	-
Tpn	0μs	-	-
Tne	0μs	-	-
Ted	0.5s	-	Discharged point @ -7.4 Volt



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8. Optical Characteristics

8-1 Specifications

Symbol	Parameter	Conditions	Temperature	Min	Typ.	Max	Unit	Note
R	Reflectance	White	25°C	30	34	-	%	Note 8-1
CR	Contrast Ratio	-	25°C	15	22	-	-	-
T _{update}	Update time	-	25°C	-	12	-	sec	-

Symbol	Parameter	Conditions	Temperature	L* Typ.	a* Typ.	b* Typ.	ΔE2000 Max.	Note
WS	White State L*/a*/b* value	White	25°C	66.5	-4	0	6	Note 8-1
DS	Dark State L*/a*/b* value	Dark	25°C	12	7	-11	6	Note 8-1
RS	Red State L*/a*/b* value	Red	25°C	26.5	41	30	6	Note 8-1
YS	Yellow State L*/a*/b* value	Yellow	25°C	62	-11	65	6	Note 8-1
BS	Blue State L*/a*/b* value	Blue	25°C	34	3.5	-37	6	Note 8-1
GS	Green State L*/a*/b* value	Green	25°C	35	-22	15	8	Note 8-1

WS: White state, DS: Dark state, RS: Red state, YS: Yellow state, BS: Blue state, GS: Green state

Note 8-1 : Luminance meter : Eye - One Pro3 plus Spectrophotometer

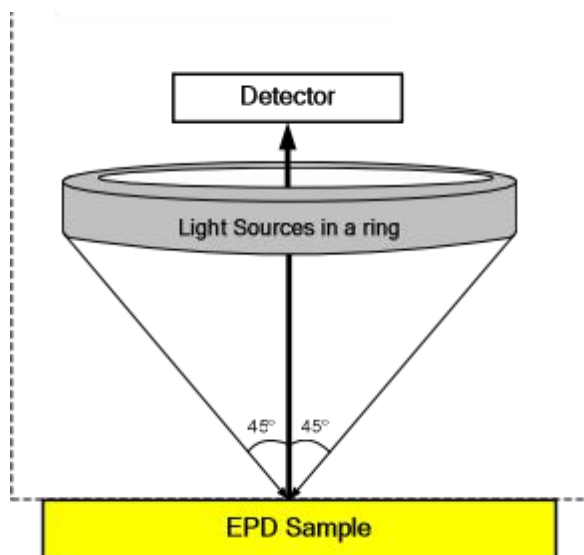


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8-2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd) :

$$CR = Rl/Rd$$



8-3 Reflection Ratio

The reflection ratio is expressed as :

$$R = \text{Reflectance Factor white board} \times (L_{\text{center}} / L_{\text{white board}})$$

L_{center} is the luminance measured at center in a white area ($R=G=B=1$). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



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9. Handling, Safety, and Environment Requirements and Remark

WARNING
The display may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Mounting Precautions
(1) It's recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It's recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
4) Acetic acid type and chlorine type materials for the cover case are not desirable because he former generates corrosive gas of attacking the PS at high temperature and the latter cause's circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.



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Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other condition these are stress ratings only

Application information

Where application information is given, it is advisory and does not form part of the specification



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10. Reliability Test

	TEST	CONDITION	REMARK
1	High Temperature Storage	T = 60°C 35% RH, 240Hrs Test in White pattern	ongoing
2	Low Temperature Storage	T = -25°C, 240Hrs Test in White pattern	ongoing
3	High Temperature Operation	T = 50°C 30% RH, 240Hrs 150s interval between updates	ongoing
4	Low Temperature Operation	T = 0°C, 240Hrs 150s interval between updates	ongoing
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90%, 240Hrs 150s interval between updates	ongoing
6	High Temperature, High-Humidity Storage	T = 60°C 80% RH, 240Hrs Test in White pattern	ongoing
7	Heat Shock	-25°C(30 min) ~60°C(30 min) 50 cycle, 1Hr/cycle Test in White pattern	ongoing
8	Electrostatic Discharge	(Machine model) +/- 200V ; 0Ω, 200pF	ongoing

Actual EMC level to be measured on customer application.

Note:

1. The protective film must be removed before temperature test.
2. For operation test, image update interval time 150s

< Criteria >

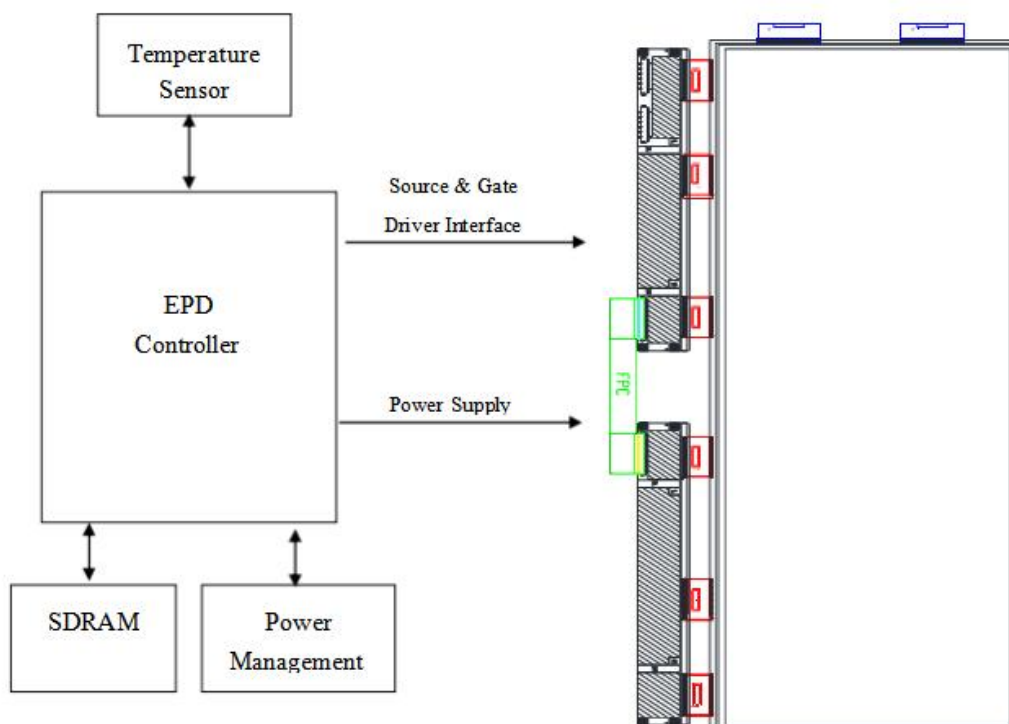
In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

3. Reliability verification of new products is ongoing, and this reliability condition is not considered as a final reliability result



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11. Block Diagram





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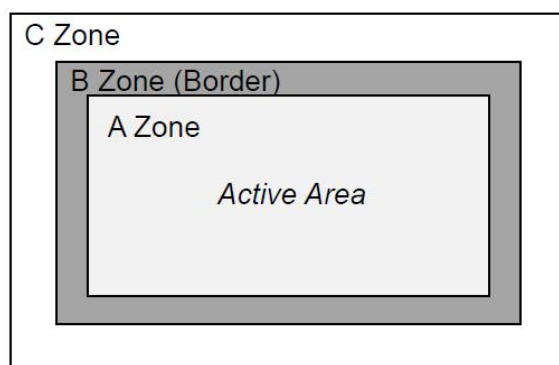
12. Shipment inspection specification

12.1 Zone Definition

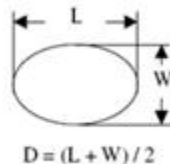
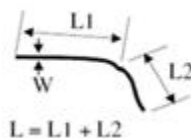
A Zone: Active Area

B Zone: Border Area

C Zone: From B Zone edge to panel edge



12.2 Line/Spot defect size





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12.3 Point and line standard

Shipment Inspection Standard						
Equipment: Electrical test fixture, Point gauge						
Outline dimension	208.8 (H) x 284.7 (V) x 0.85(D)	Unit: mm	Part-A	Active area	Part-B	Border area
Environment	Temperature	Humidity	illuminance	Distance	Time	Angle
	19℃~25℃	50±5%RH	1000~1500Lux	300 mm	35Sec	45°
Defect type	Inspection method	Standard		Part-A	Part-B	
Spot	Electric Display	D≤0.35 mm		Ignore	Ignore	
		0.35 mm<D≤0.52 mm		N≤10	Ignore	
		0.52 mm<D≤0.65 mm		N≤3	Ignore	
		D>0.65 mm		Not Allow	Ignore	
Display malfunction	Electric Display	Not Allow		Not Allow	Ignore	
Display error	Electric Display	Not Allow		Not Allow	Ignore	
Scratch or line defect(include dirt)	Visual/Film card	L≤2 mm, W≤0.1 mm		Ignore	Ignore	
		1.0mm<L≤9.0mm, 0.1<W≤0.2mm, DS>20mm		N≤2	Ignore	
		L>9.0 mm, W>0.2 mm		Not Allow	Ignore	
PS Bubble	Visual/Film card	D≤0.4mm		Ignore	Ignore	
		0.4mm≤D≤0.6mm, DS>10mm		N≤4	Ignore	
		D>0.6 mm		Not Allow	Ignore	
Corner /Edge chipping	Visual/Film card	It shall not affect the electrode circuit. The edge of the chipped corner shall be ≤ 8mm; The length X ≤ 8mm, the width Y ≤ 1mm. There shall be no cracks, and it shall not be an acute angle. And it shall not affect the electrode circuit. Only one such defect is allowed on each side.				
						
TFT warping						
Remark	1.Cannot be defect & failure cause by appearance defect;					
	2.Cannot be larger size cause by appearance defect;					



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	L=long W=wide D=point size N=Defects NO		
Mura	Refer to limit samples defined by E-INK		

12.4 Barcode



What is the QR code after picture being scanned and read? It consist of 30 numbers and letters, here is explanation for it.

QR Code: ABBBBBBBBBBFFCCCDDDEEEEGHIJKKLL

- ① A means Factory code, e.g.: H (HINK)
- ② BBBBBBBBBB refers to product model name, which is in consistent with specification part number. E.g.: E0213A189 or E0266A120; when the total code is less than 9, it would be added suffix with **. e.g.: E027A45** or E0154A78*
- ③ FF means production workshop
- ④ CCC means date of production
- ⑤ DDD means production batch
- ⑥ EEEE means FPL lot
- ⑦ G means MP/Sample/Trial/Repair
- ⑧ HIJ:(H——TFT;I——PS;J——EC Glue)
- ⑨ KK means IC type
- ⑩ LL means serial number



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13. Packing

Full carton: 12 pcs tray with products and 1 pcs empty tray.

Last carton: less 12pcs tray with products and 1 pcs empty tray. The packager will add the right amount of EPE to box so that the added EPE's height approximately close to the EPE height around the inside of the box.

